REV	DESCRIPTION	DATE	APPR
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PRELIMINARY

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PRO-LOG CORPORATION

R.L. KIMBALL 5-16-80

LITERATURE, USER' MANUAL

7603 TTL INPUT PORT CARD

A	10666A	REV A	SHT 1 OF 13

FORM NO. 101327

7603 TTL INPUT PORT CARD USER'S MANUAL

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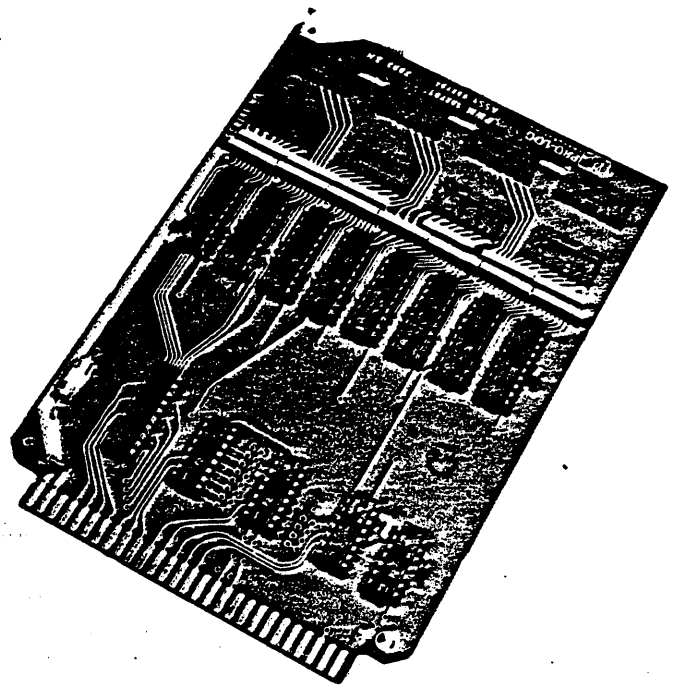
7603 INPUT PORT CARD

TTL INPUT PORT CARD

This card provides eight 8-bit gated input ports (64 input lines).

Input port lines are accessed at 16-pin DIP sockets on the card. The input lines are TTL compatible with an input rating of 4 low-power Schottky TTL loads.

The 7603 decodes eight address lines with provision for expansion and memory mapping. An on-card jumper system allows users to establish the eight consecutive input port addresses occupied by the 7603.



FEATURES

- **User selectable port address (256 port field)**
- **Input rating of 4 low-power Schottky TTL loads.**
- **Provision for expansion and memory mapping**
- **Input buffers have 200 MV of hysteresis**
- **Input lines include 4.7K pullups**
- **All IC's socketed**
- **Single +5V operation**

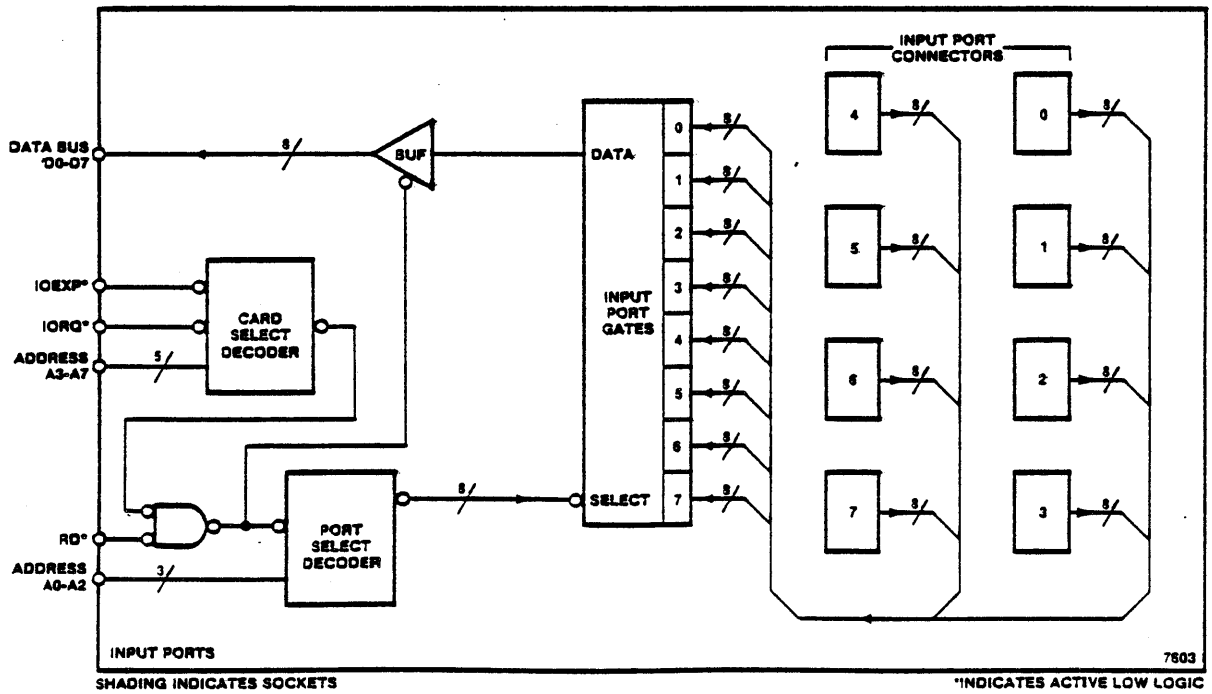


FIGURE 1

2. FUNCTIONAL DESCRIPTION

The 7603 provides 64 TTL Input lines which are alternated with 64 ground lines. These signal lines, if driven by standard LSTTL gates and with proper electrical considerations, can be up to 10 feet (3.05m) long.

When reading from an eight bit input port the state of the input lines at the time of the read is transferred to the data bus.

GENERAL PURPOSE INTERFACE

The 7603 is useful as a general purpose TTL interface card. If flat cable or twisted pair discrete wire cable assemblies are used, the ground-signal-ground of the input connectors minimizes crosstalk between inter-system signal lines in electrically noisy environments.

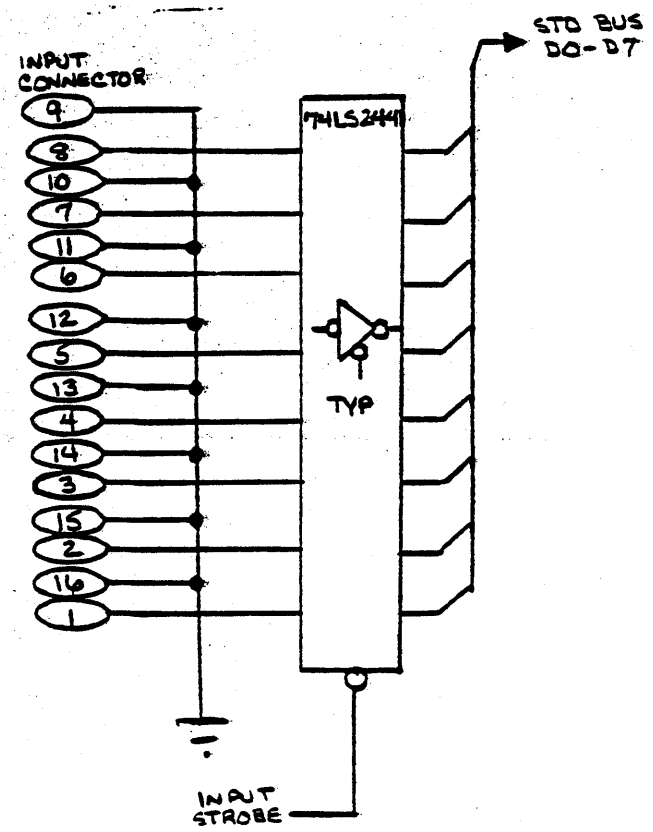


FIGURE 2 - TYPICAL INPUT PORT CIRCUIT

3. **Card Address Mapping**
The 7603 card is selected by a decoded combination of address lines A3-A7. The user chooses the card address combination by connecting one jumper wire each from SX and SY to pad matrices adjacent to U2 and U3 (See Diagram). The 7603 is shipped with Port address 00-07 Hexadecimal. To map the 7603 anywhere in the hexadecimal port address of 00-FF change the decoder outputs connected to SX and SY.

Port Addresses
Address lines A0, A1 and A2 select one of eight sequential input port addresses. The RD* input controls the input gating function.

4. ADDRESS DECODER OPERATION
Refer to the schematic, document #102793.
The 7603 uses two cascaded 74LS42 decoders (U2 and U3) to decode address lines A3-A7. These decoders are enabled only when IORQ* and IOEXP* are active. Address lines A0, A1, A2 and the RD* signal are used to gate the select strobes (which control the input ports) from U4.

CHANGING THE 7603 PORT ADDRESS
Refer to the assembly diagram, document #102794.
Locate decoders U2 and U3 (74LS42) adjacent to the STD Bus edge connector. Each decoder device has a dual row of pads which form decoder output select matrices. Make one (and only one) connection to each of the matrices adjacent to U2 and U3.

The decoder jumper pads numbered as shown in Figure 3 are adjacent to the decoder chips on the 7603. Also shown are the jumpers (at X0 and Y0) which produce hexadecimal port addresses 00, 01, 02 thru 07, the selections made when the card is shipped.

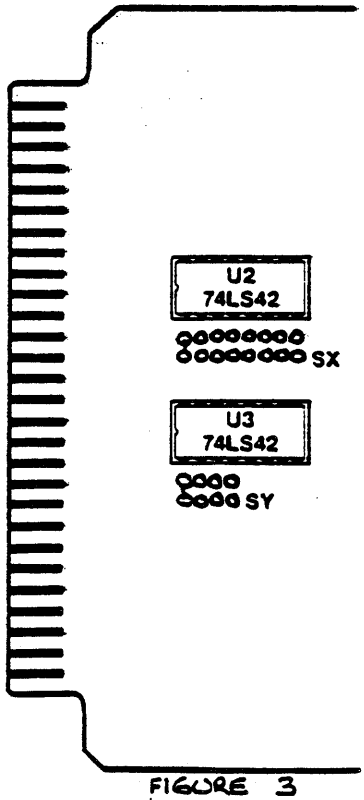


FIGURE 3
Card Address Selection

The I/O address mapping and jumper selection table for 8 addresses per card shows where to place jumper straps to obtain any eight sequential port addresses in the hexadecimal range 00-FF. Using the lower of the 2-digit hexadecimal addresses desired, find the most significant hexadecimal address digit along the verticle axis, and the least significant hex digit on the horizontal axis. For example, port addresses 00, 01, 02 thru 07 are obtained by connecting jumpers at X0 and Y0.

The only restriction that applies in address selection for the 7603 is the lower of the eight port addresses (00 as shipped) must occur only at every eighth possible address. For example, the sequence 01, 02, 03 thru 08 is not allowed by the decoder.

The pad matrices adjacent to U2 and U3 are on 0.10 inch (0.25 cm) centers. The jumper wires may be conveniently replaced by wirewrap post if frequent address selection changes are anticipated.

MOST SIGNIFICANT HEX ADDRESS	LEAST SIGNIFICANT HEX ADDRESS																JUMPER SELECTION
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	X0 Y0								X0 Y1								X AND Y
1	X0 Y2								X0 Y3								
2	X1 Y0								X1 Y1								
3	X1 Y2								X1 Y3								
4	X2 Y0								X2 Y1								
5	X2 Y2								X2 Y3								
6	X3 Y0								X3 Y1								
7	X3 Y2								X3 Y3								
8	X4 Y0								X4 Y1								
9	X4 Y2								X4 Y3								
A	X5 Y0								X5 Y1								
B	X5 Y2								X5 Y3								
C	X6 Y0								X6 Y1								
D	X6 Y2								X6 Y3								
E	X7 Y0								X7 Y1								
F	X7 Y2								X7 Y3								

FIGURE 4 - I/O Address Mapping And Jumper Selection Tables For 8 Addresses Per Card

5. 7603 CARD ENVIRONMENTAL SPECIFICATIONS

RECCOMENDED OPERATING LIMITS				ABSOLUTE NON-OPERATING LIMITS		
PARAMETER	MIN	TYP	MAX	MIN	MAX	UNITS
Free Air Temperature	0	25	55	-40	75	°C
Humidity (1)	5		95	0	95	%RH

(1) Non-condensing

6. ELECTRICAL SPECIFICATIONS

7603 TTL INPUT PORT CARD ELECTRICAL TEST SPECIFICATION

MNEM.	PARAMETER	RECOMMENDED OPERATING LIMITS			ABSOLUTE NON-OPERATING LIMITS		
		MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
Vcc	Supply voltage	4.75	5.00	5.25	0.0	7.00	Volt
T_A	Free air temp.	0	25	55	-40	75	°C

USER WORST CASE ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEST LIMITS

For Input Port

PARAMETER		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage	2.0			V
V_{IL}	Low level input voltage			0.7	V
	Hysteresis (VT+ — VT-)	0.2	0.4		V
for Input current each port line represents 4 LSTTL loads *					

* 1 LSTTL load = 0.4mA

STD BUS ELECTRICAL CHARACTERISTICS OVER RECOMMENDED TEST LIMITS

PARAMETER		MIN	TYP	MAX	UNITS
I_{CC}	SUPPLY CURRENT		350	525	mA
	STD BUS INPUT LOAD	See Figure 7			
	STD BUS OUTPUT DRIVE	See Figure 7			

7. MECHANICAL

- Meets all STD BUS general mechanical specifications
- May require one additional card slot width for ribbon cable access to input port sockets (connector dependent).
- Connectors use low profile 16-pin DIP plugs with heavy duty pins. T and B Ansley Catalog No. 609-M165H or equivalent.

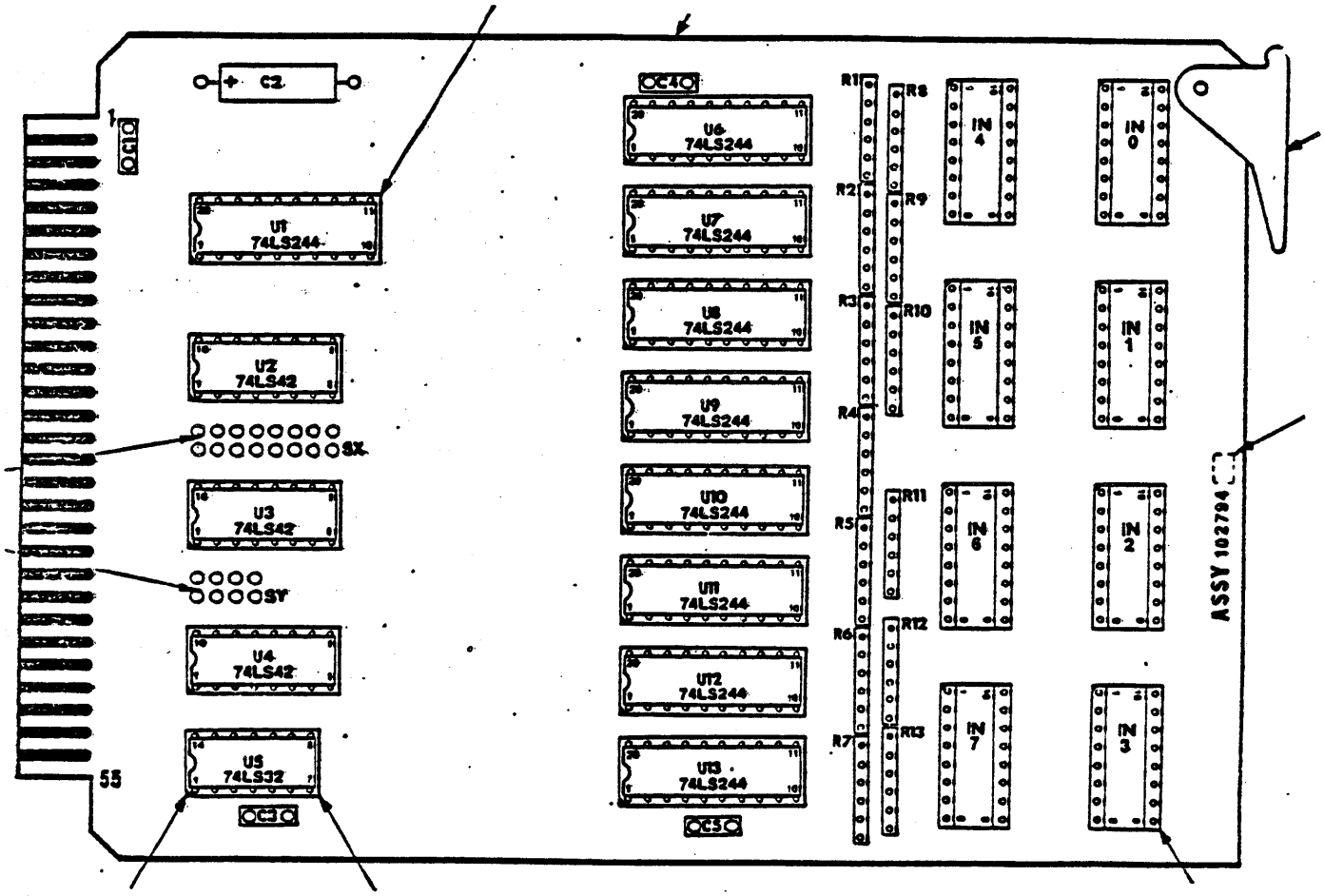


FIGURE 5 - 7603 ASSEMBLY

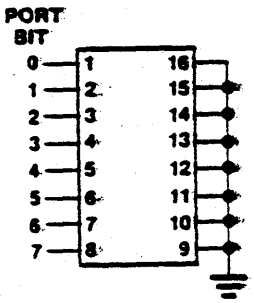


FIG. 6 - Input Port Socket

STD/7603 EDGE CONNECTOR PIN LIST							
PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)**	MNEMONIC		PIN NUMBER	OUTPUT (DRIVE)	INPUT (LOADING)**	MNEMONIC
-5 VOLTS	VCC		2		1		VCC	-5 VOLTS
GROUND	GND		4		3		GND	GROUND
-5V			6		5			-5V
D7		55	8		7	55		D3
D6		55	10		9	55		D2
D5		55	12		11	55		D1
D4		55	14		13	55		D0
A15			16		15		1	A7
A14			18		17		1	A6
A13			20		19		1	A5
A12			22		21		1	A4
A11			24		23		1	A3
A10			26		25		1	A2
A9			28		27		1	A1
A8			30		29		1	A0
RD*	1		32		31			WR*
MEMRQ*			34		33		1	IORQ*
MEMEX*			36		35		1	IOEXP*
MCSYNC*			38		37			REFRESH*
STATUS 0*			40		39			STATUS 1*
BUSRQ*			42		41			BUSAK*
INTRQ*			44		43			INTAK*
NMIRQ*			46		45			WAITRQ*
PBRESET*			48		47			SYSRESET*
CNTRL*			50		49			CLOCK*
PCI	IN		52		51	OUT		PC0
AUX GND			54		53			AUX GND
AUX -V			56		55			AUX -V

*Designates Active Low Level Logic

** Designates LSTTL Loads

FIGURE 7 - Edge Connector Pin List

7603 OPERATING SUBROUTINE MODULE

This section provides a flow diagram and subroutine to operate your 7603 card. It may be used intact, or used as a model to construct subroutines for a specific application.

The subroutine is written in 8080-family assembly code and will execute on 8080, 8085, and Z80 processors. The memory addresses selected are compatible with Pro-Log's 7801 (8085A) and 7803 (Z80) processor cards. The 7603 port addresses used are the address jumper selections made when the 7603 is shipped.

To use the subroutine in systems other than those described above, the memory and/or I/O port addresses may require change for compatibility.

The flow diagram presented can be easily translated into the assembly code used by any microprocessor since they show the steps required to achieve 7603 operation without reference to a particular microprocessor.

The following subroutine will compare the present port status with the port status from the last time that the port was read.

To use the routine the HL pointer must point to a place in memory where port status is stored. Also, the port must be read into the accumulator before calling the routine.

Upon return from the routine the location that the HL pointer was previously set will contain new port status. Plus the next four locations will contain change status.

Uses Registers A, H and L

M	XX New Data	← Location HL was set to
M + 1	XX Old Data	
M + 2	XX Changes	
M + 3	XX Bits to Zero	
M + 4	XX Bits to One	

Memory after Return

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PROGRAM ASSEMBLY FORM

TITLE 7603 DATE

HEXADECIMAL PAGE ADR	HEXADECIMAL LINE ADR	HEXADECIMAL INSTR.	MNEMONIC LABEL	MNEMONIC INSTR.	MNEMONIC MODIFIER	COMMENTS
	0			LDPI	HL	SET POINTER
	1			-	XX	
	2			-	XX	
	3			IPA		INPUT NEW DATA
	4			-	XX	
	5	46	(CHECK BITS)	LDB	M(HL)	←PUT OLD DATA IN B
	6	77		STAN	(HL)	←STORE NEW DATA
	7	23		ICP	(HL)	STORE OLD DATA IN NEXT LOCATION
	8	70		STBN	(HL)	
	9	A8		XRA	B	←OLD ⊕ NEW = CHANGES
	A	23		ICP	HL	STORE CHANGES IN NEXT LOCATION
	B	77		STAN	(HL)	
	C	4F		LDC	A	PUT CHANGES IN C
	D	78		LDA	B	PUT OLD DATA IN A
	E	A1		ANA	C	OLD • CHANGES = BITS TO ZERO
	F	23		ICP	HL	STORE BITS TO ZERO IN NEXT LOCATION
	0	77		STAN	(HL)	
	1	78		LDA	B	COMPLEMENT OLD DATA
	2	2F		CMA		
	3	A1		ANA	C	$\overline{OLD}$ • CHANGES = BITS TO ONE
	4	23		ICP	HL	STORE BITS TO ONE IN NEXT LOCATION
	5	77		STAN	(HL)	
	6	C9		RTS	UN	RETURN FROM SUBROUTINE
	7					USES REGS A, B, C, H AND L
	8					
	9					
	A					
	B					
	C					
	D					
	E					
	F					

```
00001111 OLD
⊕01011010 CHANGE
01011010 CHANGE
```

```
00001111 OLD
• 01011010 CHANGE
00001010 BITS TO ZERO
```

```
11110000 OLD
• 01011010 CHANGE
01010000 BITS TO ONE
```

RAM MEMORY AFTER RETURN (USES 5 LOCATIONS)	XX NEW DATA
	XX OLD DATA
	XX CHANGES
	XX BITS TO ZERO
	XX BITS TO ONE

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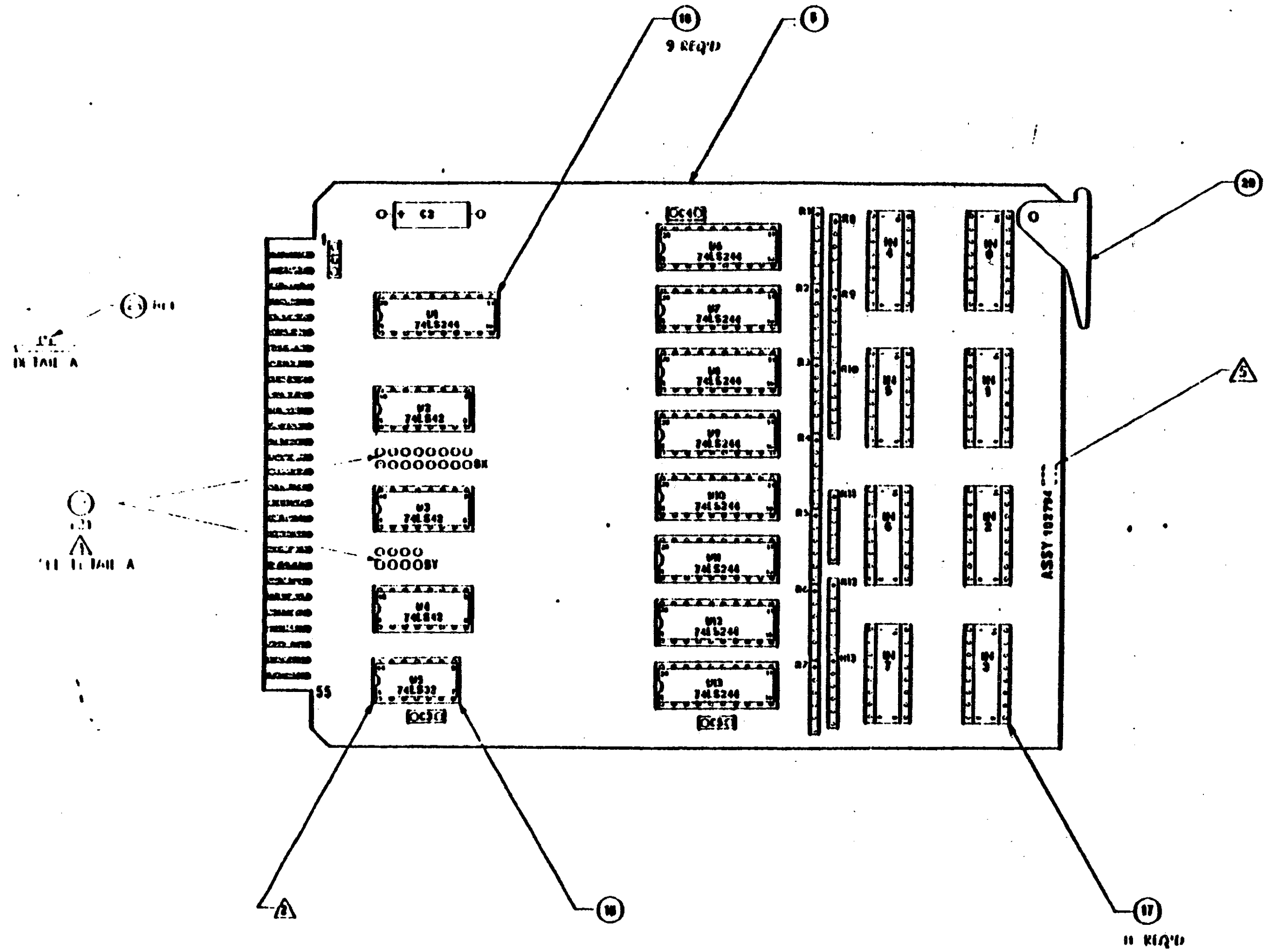

REVISIONS				
LTR	DESCRIPTION		DATE	APPR
B	REVISED PER ECN 684.			

REFERENCE ONLY

ITEM	DESCRIPTION	REF DESIGNATION
10	47K NETWORK	R1-R13
9		
8	33 uF 50V	C1, C3-C5
7	10 uF 25V	C2

PRO-LOG CORPORATION

ASSEMBLY 7603 INPUT GATE CARD

C.A. CLARK

D 102734 C

SCHEMATIC NO 102798
PARTS LIST NO 102795

5. IDENTIFY WITH ASSEMBLY REV LETTER USING RUBBER STAMP.

4. REF DESIGNATIONS ARE FOR LOCATING PURPOSES ONLY AND MAY NOT APPEAR ON ACTUAL PART.

3. [illegible]

2. INDICATES PIN NO 1 OF SOCKETS (TYP).

1. FOR ASSY PROCEDURES SEE AS1004.

NOTES: UNLESS OTHERWISE SPECIFIED.

101356

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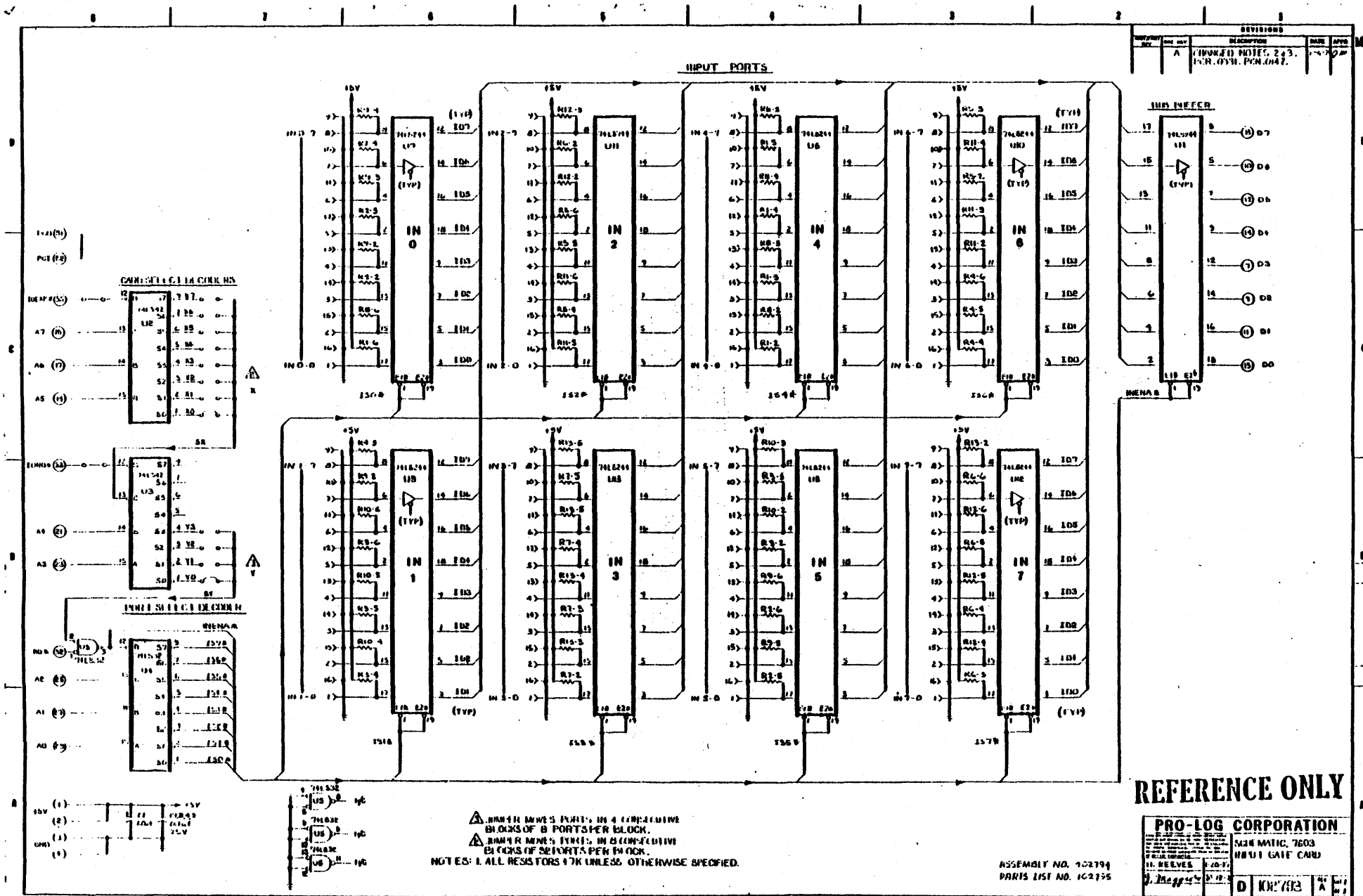

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