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This book describes Harris Semiconductor Products Division's complete line of microprocessor products and includes a complete set of product specifications and data sheets. Also included are sections on support systems, reliability, and packaging.

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NOTE: *Available as separate data sheets.

## Data Sheet Classifications

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<td>Advance Information DATA SHEET</td>
<td>Sampling or Pre-Production</td>
<td>This is advanced information, and specifications are subject to change without notice.</td>
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<td>First Production</td>
<td>Supplementary data maybe published at a later date. Harris reserves the right to make changes anytime without notice, in order to improve design and supply the best product possible.</td>
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CMOS Microprocessor Products

GENERAL DESCRIPTION

The 6100 CMOS Microprocessor Family offers all CMOS components, enabling the designer to build low power PDP-8 based microcomputer systems. Obvious advantages of this architecture are readily available software, a variety of development and operating systems and a familiar instruction set that is easy to program. The low power, single voltage CMOS circuitry and LSI design of each component within the 6100 microcomputer system will result in cost effective systems that minimize power and packaging costs. For example, the operating power drain for a system consisting of 256 words of RAM, an interval timer, two latched I/O ports, an I/O controller, and 1024 words of ROM is typically less than 100mW. Minimum package, high density configurations allow this all CMOS microcomputer to be incorporated on small printed circuit boards (approximately 4” by 5”), suggesting interesting possibilities for portable, self-contained equipment designs. Here are a few of the benefits derived from the 6100 microcomputer system.

- Battery operation
- Data retention during power outages
- Data acquisition at remote sites
- On-site data reduction
- Portable systems
- Remote instrumentation
- Small size, low cost

The microprocessor family components include a 12-bit CPU, various I/O controllers and a wide variety of CMOS memory and bus driver devices. Using just a few of these LSI components, a minimum yet very powerful microcomputer, as shown in Figure 1, can be built having the following features.

- ROM – 1024 x 12
- RAM – 64 x 12
- Vectored or polled I/O interrupts
- Four programmable outputs
- Control for two I/O ports

The complete 6100 microprocessor product line is tabulated in Tables 1, 2, 3, and 4. For parametric data consult the appropriate product data sheet.

Figure 1 – Minimum CMOS Microcomputer
### Table 1 — CMOS Microprocessor Products

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* Digital Equipment Corporation Trademark
System Architecture

Figure 2 shows the architecture of an HM-6100 system. Note that the Register Page and Auto Increment Registers which are an integral part of the processor architecture are located in memory rather than "on-chip". This permits a larger number of registers to be made available (128 per field) and they can be operated on by all Memory Reference Instructions rather than a separate group of "register operation" instructions.

The registers on the register page are true general purpose registers in that they can be accessed with a single word instruction from anywhere in the instruction field, and can be used as stack pointers, program vectors, or as memory locations.

**CONTROL PANEL MEMORY**
- Register Page = 0-177
- Auto Increment Register = 10-17
- CP Interrupt PC Storage = 0000
- First Instruction of CP Interrupt = 7777
- 4K, 12-Bit Words

**MICROPROCESSOR**
- Accumulator (AC)
- Link (L)
- Multiplier Quotient (MQ)
- Program Counter (PC)
- Memory Address Register (MAR)
- Instruction Register (IR)

**MAIN MEMORY**
- Register Page = 0-177
- Auto Increment Register = 10-17
- Interrupt PC Storage = 0000
- First Instruction of Interrupt = 0001
- First Instruction after Reset = 7777
- 4K, 12-Bit Words per Field
- Expandable to 8 Fields

**INPUT/OUTPUT UNITS**
- Switch Register (SW)
- 63 I/O Devices
- Program Data Transfer
- Program Interrupt Transfer
- Direct Memory Access

Figure 2 — HM-6100 System Architecture

Microprocessor Features

Since the HM-6100 bridges the gap between the microprocessor and minicomputer worlds, it has some features not found in most 8-bit microprocessors. These are explained more fully in the HM-6100 data sheet, but briefly they are:

**Memory Reference Instructions (MRIs)** — Combine the operation and the address of the operand in a single memory word. This eliminates the requirement for "immediate" instructions, shortens programs significantly, and speeds execution.

**Memory Fields and Pages** — The 32K memory space is conceptually divided into 4K word fields which are subdivided into 128 word pages. The memory reference instruction addresses are always specified relative to the beginning of a specific page, thus making software "page relocatable".
General Purpose Registers Located in Memory — The first 128 words of each memory field (page 0, or the Register Page) can be used as general purpose registers. Since they are located in memory, the MRIs are used to manipulate them rather than a separate set of "register instructions".

Auto Increment Registers — When locations 10-178 of the register page are used as operand addresses they are automatically incremented prior to each use.

IOTs — There is an entire class of Input/Output transfer instructions. Hardware interfacing of the CPU to the various peripherals is simple and straightforward.

Microcode — Accumulator operations can be microcoded to tailor the instruction set to a particular application.

Execution Times — Since the HM-6100 is a static device which can be operated at clock frequencies from 0 to 8MHz, the number of states required to execute each instruction is given.

Control Panel Memory — This has been included in the HM-6100 to simplify implementation of the control panel function in microcomputer systems. Its use is not, however, limited to that function in that the control panel interrupt request is a true non-maskable interrupt which accesses a program stored in Control Panel (CP) memory. As such, CP memory is valuable for functions such as system debug, system diagnostic programs, non-maskable interrupt routines, resident storage of frequently used for software, etc. It is in no way limited to "Control Panel Functions". The HM-6100 will execute programs in Control Panel Memory or Main Memory or a combination of both.

NOTE: In HM-6100 literature bit 0 refers to the MSB, bit 11 refers to the LSB. Data is represented in Two’s Complement Integer notation. In this system, the negative of a number is formed by complementing each bit in the data word and adding “1” to the complemented number. The sign is indicated by the most significant bit. In the 12-bit word used by the HM-6100, when bit 0 is a “0”, it denotes a positive number and when bit 0 is a “1”, it denotes a negative number. The maximum number ranges for this system are 37778 (+2047) and 40008 (-2048).

System Flexibility

Using the HM-6100 family, the designer has access to a comprehensive product line dedicated to satisfy his particular system requirements. He also has a very low cost reproduction of the PDP-8/E minicomputer whose existence is justified by a large product market base and a wealth of existing software. The wide range of CMOS memory products enable partitioning of the memory system in blocks from 64 to 4096 words of RAM and from 256 to 1024 words of ROM or PROM.

DEVELOPMENT SUPPORT

The 6100 CPU family is supported by the Harris, single-board, CMOS MICRO-12 microcomputer and by existing PDP-8 minicomputers and their low cost operating systems.
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Features

- LOW POWER - TYP. < 5.0μW STANDBY
- SINGLE SUPPLY 4-11 VOLT
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- SINGLE PHASE CLOCK, ON CHIP CRYSTAL OSC.
- SOFTWARE COMPATIBLE WITH PDP-8/E
- 12-BIT DATA WORD
- OVER 90 SINGLE WORD INSTRUCTIONS
- RELOCATABLE MEMORY ORGANIZATION
- BASIC ADDRESSING TO 4K 12 BIT WORDS
- PROVISION FOR DEDICATED CONTROL PANEL
- 128 GENERAL PURPOSE REGISTERS
- 8 AUTOINDEXING REGISTERS
- FLEXIBLE PROGRAMMED I/O TRANSFERS
- VECTORED INTERRUPT CAPABILITY

Description

The HM-6100 is a single address, fixed word length, parallel transfer microprocessor using 12-bit two’s complement arithmetic. It is a general purpose processor which recognizes the instruction set of Digital Equipment Corporation’s PDP-8/E Minicomputer.

Standard features include indirect addressing and facilities for instruction skipping, program interrupts as a function of input/output device conditions, and auto-restart. Five 12-bit registers are used to control microprocessor operations, address memory, perform arithmetic or logical operations, and store data. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

Pinout

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<tr>
<th>VCC</th>
<th>1</th>
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<td>CPSEL</td>
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<td>36</td>
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<td>35</td>
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<td>18</td>
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Functional Diagram
Specifications HM-6100A

**ABSOLUTE MAXIMUM RATINGS**

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<tr>
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<th>Min</th>
<th>Typ</th>
<th>Max</th>
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<tbody>
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<td>Input or Output Voltage Applied</td>
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<tr>
<td>Storage Temperature Range</td>
<td>-65°C to 150°C</td>
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</tr>
<tr>
<td>Operating Temperature Range</td>
<td>Industrial HM-6100A-9</td>
<td>-40°C to +85°C</td>
<td></td>
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<tr>
<td></td>
<td>Military HM-6100A-2</td>
<td>-55°C to +125°C</td>
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**ELECTRICAL CHARACTERISTICS**

VCC = 10.0 ± 0.5 Volts, TA = Industrial or Military

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<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
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<td>V</td>
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<tr>
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**Notes:**
(1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

---

**A.C.**

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<th>SYMBOL</th>
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<th>MIN</th>
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</tbody>
</table>

**NOTE 1:**
All devices guaranteed at worst case limits. Room temperature, 10V data provided for information - not guaranteed.
## Specifications HM-6100

### Absolute Maximum Ratings

- **Supply Voltage**
  - +8.0V
- **Input or Output Voltage Applied**
  - Gnd -0.3V to VCC +0.3V
- **Storage Temperature Range**
  - -65°C to +150°C
- **Operating Temperature Range**
  - Industrial HM-6100-9: -40°C to +85°C
  - Military HM-6100-2: -55°C to +125°C

### Electrical Characteristics

For VCC = 5.0 ± 10% Volts, TA = Industrial or Military

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
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<td>VIH</td>
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<td>70% VCC</td>
<td></td>
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<td>V</td>
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<td>V</td>
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<td>VIL</td>
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<td>20% VCC</td>
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<td>V</td>
<td></td>
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<td>Logical &quot;0&quot; Osc. Input Voltage</td>
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<td>V</td>
<td></td>
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<td>µA</td>
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<td></td>
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**Notes:**
1. Except pin 14 and 15
2. Except pin 14
3. Guaranteed and sampled, but not 100% tested.

### Test Conditions

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
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<tr>
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<td>MHz</td>
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<tr>
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**NOTE 1:** All devices guaranteed at worst case limits. Room temperature, 5V data provided for information - not guaranteed.
Specifications HM-6100C-9

Absolute Maximum Ratings

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<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>8.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>Gnd -0.3V to VCC +0.3V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to 150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Electrical Characteristics VCC = 5.0 ± 5% Volts, TA = Industrial

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIHC</td>
<td>Logical &quot;1&quot; Osc. Input Voltage</td>
<td>VCC-.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VILC</td>
<td>Logical &quot;0&quot; Osc. Input Voltage</td>
<td>GND+.5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage (1)</td>
<td>-10</td>
<td></td>
<td>+10</td>
<td>µA</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Volt. (2)</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Volt. (2)</td>
<td>0.45</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-10</td>
<td></td>
<td>+10</td>
<td>µA</td>
</tr>
<tr>
<td>ICC1</td>
<td>Supply Current (Static)</td>
<td>600</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>ICC2</td>
<td>Supply Current (Operating)</td>
<td>5.0</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance (3)</td>
<td>5</td>
<td></td>
<td>7</td>
<td>pF</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance (3)</td>
<td>8</td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CIO</td>
<td>Input/Output Capacitance (3)</td>
<td>8</td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>COSC</td>
<td>Oscillator IN/OUT CAP. (3)</td>
<td>30</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

Notes: (1) Except pin 14 and 15
(2) Except pin 14
(3) Guaranteed and sampled, but not 100% tested.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>fMAX</td>
<td>Max operating Freq.</td>
<td>3.33</td>
<td>2.5</td>
<td>MHz</td>
</tr>
<tr>
<td>TS</td>
<td>Major State Time</td>
<td>600</td>
<td>800</td>
<td>ns</td>
</tr>
<tr>
<td>TLX</td>
<td>LXMAR Pulse Width</td>
<td>270</td>
<td>335</td>
<td>ns</td>
</tr>
<tr>
<td>TAS</td>
<td>Address Setup Time</td>
<td>100</td>
<td>120</td>
<td>ns</td>
</tr>
<tr>
<td>TAH</td>
<td>Address Hold Time</td>
<td>150</td>
<td>175</td>
<td>ns</td>
</tr>
<tr>
<td>TAL</td>
<td>Access Time from LXMAR</td>
<td>600</td>
<td>650</td>
<td>ns</td>
</tr>
<tr>
<td>TEN</td>
<td>Output Enable (Memory)</td>
<td>300</td>
<td>400</td>
<td>ns</td>
</tr>
<tr>
<td>TEND</td>
<td>Output Enable (I/O)</td>
<td>350</td>
<td>575</td>
<td>ns</td>
</tr>
<tr>
<td>TWP</td>
<td>Write Pulse Width</td>
<td>250</td>
<td>320</td>
<td>ns</td>
</tr>
<tr>
<td>TDS</td>
<td>Data Setup (Memory)</td>
<td>180</td>
<td>240</td>
<td>ns</td>
</tr>
<tr>
<td>TDSD</td>
<td>Data Setup (I/O)</td>
<td>200</td>
<td>275</td>
<td>ns</td>
</tr>
<tr>
<td>TDH</td>
<td>Data Hold Time</td>
<td>130</td>
<td>175</td>
<td>ns</td>
</tr>
<tr>
<td>TST</td>
<td>Status Signals Valid</td>
<td>300</td>
<td>350</td>
<td>ns</td>
</tr>
<tr>
<td>TRS</td>
<td>Request Inputs Setup</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>TRH</td>
<td>Request Inputs Hold</td>
<td>100</td>
<td>130</td>
<td>ns</td>
</tr>
<tr>
<td>TWS</td>
<td>Wait Setup Time</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>TWH</td>
<td>Wait Hold Time</td>
<td>100</td>
<td>130</td>
<td>ns</td>
</tr>
<tr>
<td>TRHS</td>
<td>Run Halt Setup Time</td>
<td>0</td>
<td>70</td>
<td>ns</td>
</tr>
<tr>
<td>TRHP</td>
<td>Run Halt Pulse Width</td>
<td>100</td>
<td>130</td>
<td>ns</td>
</tr>
</tbody>
</table>

Note 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information - not guaranteed.
Timing and State Control

The HM-6100 generates all the timing and state signals internally. A crystal is used to control the CPU operating frequency. The CPU divides the crystal frequency by two. With a 4MHz crystal, the internal states will be of 500ns duration. The major timing states are described in Figure 1.

T1 For memory reference instructions, a 12-bit address is sent on the DataX, DX, lines. The Load External Address Register, LXMAR, is used to clock an external register to store the address information externally, if required. When executing an Input-Output I/O instruction, the instruction being executed is sent on the DX lines to be stored externally. The external address register then contains the device address and control information.

Various CPU request lines are priority sampled if the next cycle is an Instruction Fetch cycle. Current state of the CPU is available externally.

T2 Memory/Peripheral data is read for an input transfer (READ). WAIT controls the transfer duration. If WAIT is active during input transfers, the CPU waits in the T2 state. The wait duration is an integral multiple of the crystal frequency - 250ns for 4MHz.

For Memory reference instructions, the Memory Select, MEMSEL, lines are active. For I/O instruction the DEVSEL, line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines C0, C1, C2, and SKP are sampled if the instruction being executed is an I/O instruction.

Control Panel Memory Select, CPSEL, and Switch Register Select, SWSEL, become active low for data transfers between the HM-6100 and Control Panel Memory and the Switch Register, respectively.

T3, T4, T5 ALU operation and internal register transfers.

T6 This state is entered for an output transfer (WRITE). The address is defined during T1. WAIT controls the time for which the WRITE data must be maintained.

The following illustrates the timing of the CPU when its operating frequency is low enough that propagation delays can be ignored. It effectively shows the timing of the CPU when it is single clocked.

FIGURE 1 — Static Timing
The dynamic or high frequency timing illustrates the propagation delays at specified operating frequencies. (Refer to specifications) It defines the interface requirements for memory and I/O devices on the bus.

![Timing Diagram]

**FIGURE 2 — Dynamic Timing**

*Microprocessor Architecture*

The block diagram of the CPU architecture, shown on the front page, consists of the following major functional segments:

- CPU Registers
- Arithmetic and Logic Unit
- Dx-Bus Multiplexer
- Timing and Control Unit

Each one is briefly described below.

**CPU REGISTERS**

The CPU consists of five, 12-bit registers, of which three are user programmable; 1) Accumulator (AC), 2) Program Counter (PC), and 3) Multiply Quotient (MQ). The remaining two registers are the Instruction Register (IR) and the Memory Address Register (MAR) which are used exclusively for internal operations. The CPU registers are defined as follows.

**ACCUMULATOR AND LINK (AC/L)**

All arithmetic and logical operations are performed in the AC. For any arithmetic operation, the AC data and memory data are combined in the ALU and the result is temporarily stored in the AC. Under software control, the AC can be cleared, set, complemented, incremented, tested or rotated. Using the Operate Microinstructions, a variety of register operate instructions can be derived.

The link is a one-bit extension of the AC. It can be complemented with a carry out of the ALU or cleared, set, complemented, tested and rotated along with the rest of the AC. It also serves as the carry output for two’s complement arithmetic.

**MULTIPLY QUOTIENT (MQ)**

The MQ register can be used as a temporary storage for the AC. The MQ may be OR’ed with the AC and the result stored in the AC or the contents of the AC and MQ may be swapped. The MQ is used in conjunction with the AC to perform multiplication, division, and double-precision operations.
PROGRAM COUNTER (PC)
The PC supports both memory and input-output device operations. For memory operations, the PC is controlled exclusively by internal logic and instructions fetched from memory. During an instruction fetch cycle the contents of the PC are transferred to the memory address register (MAR) while the current instruction is being decoded. The PC is then loaded with a new address or simply incremented for the next instruction depending upon the type of instruction. The next instruction obtained from memory is then loaded into the Instruction Register. For example, if the instruction is a JMP X, then the branch address X is loaded into the PC for program controlled branching.

Branching can also be controlled by an external device during input-output operations. This feature allows I/O controlled vectored interrupts.

MEMORY ADDRESS REGISTER (MAR)
The MAR contains the address of the memory location that is currently selected for memory or I/O read-write operations. It is also used for microprogram control during data transfers to and from memory and peripherals.

INSTRUCTION REGISTER (IR)
The instruction fetched from memory is held in the IR while being interpreted by the Instruction Decoder. The IR specifies the initial step of the microprogram sequence for each instruction and is also used to store temporary data for microprogram control.

ARITHMETIC AND LOGIC UNIT (ALU)
The ALU performs 12-bit arithmetic, logical and rotate operations. Its input is derived from the AC and any one of the other CPU registers. The type of operations performed by the ALU include:

- ADD
- Logical AND
- Logical OR
- Test AC
- Left-right shifts and rotates
- Increment
- Complement
- Set/Clear

DX-BUS MULTIPLEXER
To keep the CPU pin count to a reasonable 40 and still maintain a 12-bit word structure, the address and data paths are multiplexed by the DX-Bus Multiplexer. It handles data, address and instruction transfers between the CPU and memory or peripheral devices on a time-multiplexed basis.

TIMING AND CONTROL UNIT
The Timing and Control Unit generates the state and cycle timing signals from a single-phase clock and maintains the proper sequences of events required for any processing task. It also decodes the instruction obtained from the IR and combines the result with various timing signals and external control inputs to provide control and gating signals required by other functional units (both internal and external to the CPU).

Memory Organization
The HM-6100 has a basic addressing capacity of 4096 12-bit words. The addressing capacity may be extended to 32K words by Extended Memory Control hardware. Every location has a unique 4 digit octal (12 bit binary) address, 0000g to 7777g (000010 to 409510). The Memory is subdivided into 32 PAGES of 128 words each. Memory Pages are numbered sequentially from Page 00g, containing addresses 0000-0177g, to Page 37g, containing addresses 7600g-7777g. The first 5 bits of a 12-bit MEMORY ADDRESS denote the PAGE NUMBER and the low order 7 bits specify the PAGE ADDRESS of the memory location within the given Page.

![Memory Organization Diagram]

FIGURE 3 - Memory Organization
Memory and Processor Instructions

The HM-6100 instructions are 12-bit words stored in memory. The HM-6100 makes no distinction between instruction and data; it can manipulate instructions as stored variables or execute data as instructions. There are three general classes of HM-6100 instructions. They are Memory Reference Instructions (MRI), Operate Instructions (OPR), and Input/Output Transfer Instructions (IOT).

During an instruction fetch cycle, the HM-6100 fetches the instruction pointed to by the PC. The contents of the PC are transferred to the MAR. The PC is incremented by 1. The PC now contains the address of the “current” instruction which must be fetched from memory. Bits 0-4 of the MAR identify the CURRENT PAGE, that is, the Page from which instructions are currently being fetched and bits 5-11 of the MAR identify the location within the Current Page. (PAGE ZERO (0), 0000g-0177g, by definition, denotes the first 128 words of memory and is called the Register Page.)

Since the HM-6100 is a static design it can operate at any crystal frequency from 0 to 8MHz. State times required for execution are given for each instruction. Execution time can be calculated from the equation:

\[ T = N \times (2 + (1/F)) \]

where N is the number of state times and F is the crystal or input clock frequency.

MEMORY REFERENCE INSTRUCTIONS (MRI)

The Memory Reference Instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. The first 3 bits of a Memory Reference Instruction specify the operation code, or OPCODE, and the low order 9 bits, the OPERAND address, as shown in Figure 4.

<table>
<thead>
<tr>
<th>OP CODE 0 - 5</th>
<th>IA</th>
<th>MP</th>
<th>PAGE RELATIVE ADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>IA: Indirect Addressing</td>
<td>0 = Direct; 1 = Indirect</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MP: Memory Page</td>
<td>0 = Register Page; 1 = Current Page</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

FIGURE 4 – Memory Reference Instruction Format

Bits 5 through 11, the PAGE ADDRESS, identify the location of the OPERAND on a given page, but they do not identify the page itself. The page is specified by bit 4, called the CURRENT PAGE OR REGISTER PAGE BIT. If bit 4 is a 0, the page address is interpreted as a location on the Register Page. If bit 4 is a 1, the page address specified is interpreted to be on the Current Page.

By this Method, 256 locations may be directly addressed, 128 on the REGISTER PAGE and 128 on the CURRENT PAGE. Other locations are addressed by using bit 3. When bit 3 is a 0, the operand address is a DIRECT ADDRESS. An INDIRECT ADDRESS (pointer address) identifies the location that contains the desired address (effective address). To address a location that is not directly addressable, not in the REGISTER PAGE or in the CURRENT PAGE, the absolute address of the desired location is stored in one of the 256 directly addressable locations (pointer address). Upon execution, the MRI will operate on the contents of the location identified by the address contained in the pointer location. Note that locations 0010g-0017g in the Register Page are AUTOINDEXED. When these locations are used for index registers their contents are incremented by 1 and restored before they are used as the operand address. These locations are therefore convenient for indexing applications.

Combinations of mode and page bits yield four (4) addressing modes:

- Current Page, Direct
- Current Page, Indirect
- Register Page, Direct
- Register Page, Indirect

A fifth addressing mode results from use of the AUTOINDEX registers:

- Register Page, Autoindexed
### TABLE 1

<table>
<thead>
<tr>
<th>MNE-MONIC</th>
<th>OPERAND</th>
<th>NUMBER OF STATES</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>DIRECT</td>
<td>INDIRECT</td>
</tr>
<tr>
<td>AND</td>
<td>0XXX</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>TAD</td>
<td>1XXX</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>ISZ</td>
<td>2XXX</td>
<td>16</td>
<td>21</td>
</tr>
<tr>
<td>DCA</td>
<td>3XXX</td>
<td>11</td>
<td>16</td>
</tr>
<tr>
<td>JMS</td>
<td>4XXX</td>
<td>11</td>
<td>16</td>
</tr>
<tr>
<td>JMP</td>
<td>5XXX</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>IOT</td>
<td>6XXX</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td>OPI</td>
<td>7XXX</td>
<td>10</td>
<td>15</td>
</tr>
</tbody>
</table>

#### Operate Instructions

The Operate Instructions, which have an OPCODE of 7g(111), consist of 3 groups of microinstructions. Group 1 microinstructions, which are identified by the presence of a 0 in bit 3, are used to perform logical operations on the contents of the accumulator and link. Group 2 microinstructions, which are identified by the presence of a 1 in bit 3 and a 0 in bit 11, are used primarily to test the contents of the accumulator and then conditionally skip the next sequential instruction. Group 3 microinstructions have a 1 in bit 3 and a 1 in bit 11 and are used to perform logical operations on the contents of the AC and MQ.

The basic OPR instruction format is shown in Figure 5. Operate microinstructions from any group may be microprogrammed with other operate microinstructions of the same group. The actual code for a microprogrammed combination of two, or more, microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 microinstructions performed first, logical sequence number 2 microinstructions performed second, logical sequence number 3 microinstructions performed third, and so on. Two operations with the same logical sequence number, within a given group of microinstructions, are performed simultaneously.
GROUP 1 MICROINSTRUCTIONS

Figure 6 shows the instruction format of a group 1 microinstruction. Any one of bits 4 to 11 may be set, loaded with a binary 1, to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 6.

Table 2-1 lists commonly used group 1 microinstructions, their assigned mnemonics, octal number, instruction format, logical sequence, the operation they perform, and the number of states. The same format is followed in Table 3 and 4 which corresponds to group 2 and 3 microinstructions, respectively.

There are several commonly used microprogrammed combinations of group 1 microinstructions. These are listed in Table 2-2. When writing programs it is necessary to load various constants into the AC for such purposes as initializing counters and to provide comparisons. Table 2-3 lists those constants which can be loaded directly via microprogrammed combinations of group 1 instructions.

<table>
<thead>
<tr>
<th>MNE-MONIC</th>
<th>OCTAL CODE</th>
<th>LOGICAL SEQUENCE</th>
<th>NUMBER OF STATES</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td>7000</td>
<td>1</td>
<td>10</td>
<td>NO OPERATION - This instruction causes a 10 state delay in program execution, without affecting the state of the HM-6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.</td>
</tr>
<tr>
<td>CLA</td>
<td>7200</td>
<td>1</td>
<td>10</td>
<td>CLEAR ACCUMULATOR - The accumulator is loaded with binary 0’s.</td>
</tr>
</tbody>
</table>
FIGURE 2 – 1 Continued

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>LOGICAL SEQUENCE</th>
<th>NUMBER OF STATES</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLL</td>
<td>7100</td>
<td>1</td>
<td>10</td>
<td>CLEAR LINK – The link is loaded with a binary 0.</td>
</tr>
<tr>
<td>CMA</td>
<td>7040</td>
<td>2</td>
<td>10</td>
<td>COMPLEMENT ACCUMULATOR – The content of each bit of the AC is complemented. This has the effect of replacing the contents of the AC with its one’s complement.</td>
</tr>
<tr>
<td>CML</td>
<td>7020</td>
<td>2</td>
<td>10</td>
<td>COMPLEMENT LINK – The content of the link is complemented.</td>
</tr>
<tr>
<td>IAC</td>
<td>7001</td>
<td>3</td>
<td>10</td>
<td>INCREMENT ACCUMULATOR – The content of the AC is incremented by one (1) and the carry out components the Link (L).</td>
</tr>
<tr>
<td>BSW</td>
<td>7002</td>
<td>4</td>
<td>15</td>
<td>BYTE SWAP – The right six (6) bits of the AC are exchanged or SWAPPED with the left six bits. AC(0) is swapped with AC(6), AC(1) with AC(7), etc. The link is not affected.</td>
</tr>
<tr>
<td>RAL</td>
<td>7004</td>
<td>4</td>
<td>15</td>
<td>ROTATE ACCUMULATOR LEFT – The content of the AC and L are rotated one binary position to the left. AC(0) is shifted to L and L is shifted to AC(11). The ROTATE instructions use what is commonly called a circular shift, meaning that any bit rotated off one end of the accumulator will reappear at the other end.</td>
</tr>
<tr>
<td>RTL</td>
<td>7006</td>
<td>4</td>
<td>15</td>
<td>ROTATE TWO LEFT – The contents of the AC and L are rotated two binary positions to the left. AC(1) is shifted to L and L is shifted to AC(10).</td>
</tr>
<tr>
<td>RAR</td>
<td>7010</td>
<td>4</td>
<td>15</td>
<td>ROTATE ACCUMULATOR RIGHT – The contents of the AC and L are rotated one binary position to the right. AC(11) is shifted to L and L is shifted to AC(0).</td>
</tr>
<tr>
<td>RTR</td>
<td>7012</td>
<td>4</td>
<td>15</td>
<td>ROTATE TWO RIGHT – The contents of the AC and L are rotated two binary positions to the right. AC(10) is shifted to L and L is shifted to AC(1).</td>
</tr>
</tbody>
</table>

TABLE 2 – 2

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>LOGICAL SEQUENCE</th>
<th>NUMBER OF STATES</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLA CLL</td>
<td>7300</td>
<td>1</td>
<td>10</td>
<td>CLEAR ACCUMULATOR – CLEAR LINK</td>
</tr>
<tr>
<td>CIA</td>
<td>7041</td>
<td>2, 3</td>
<td>10</td>
<td>COMPLEMENT AND INCREMENT ACCUMULATOR – The content of the AC is replaced with its two’s complement. The carry out complements the link. This is a microprogrammed combination of CMA and IAC.</td>
</tr>
<tr>
<td>STL</td>
<td>7120</td>
<td>1, 2</td>
<td>10</td>
<td>SET THE LINK – The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.</td>
</tr>
<tr>
<td>STA</td>
<td>7240</td>
<td>1, 2</td>
<td>10</td>
<td>SET THE ACCUMULATOR – Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.</td>
</tr>
<tr>
<td>CLA IAC</td>
<td>7201</td>
<td>1, 3</td>
<td>10</td>
<td>Sets the accumulator to a 1.</td>
</tr>
</tbody>
</table>
Table 2-2 Continued

<table>
<thead>
<tr>
<th>MNE-MONIC</th>
<th>OCTAL CODE</th>
<th>LOGICAL SEQUENCE</th>
<th>NUMBER OF STATES</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GLK</td>
<td>7204</td>
<td>1, 4</td>
<td>15</td>
<td>GET LINK - The AC is cleared and the content of the link is shifted into AC(11) while a 0 is shifted into the link. This is a microprogrammed combination of CLA and RAL.</td>
</tr>
<tr>
<td>CLL RAL</td>
<td>7104</td>
<td>1, 4</td>
<td>15</td>
<td>CLEAR LINK - ROTATE ACCUMULATOR LEFT</td>
</tr>
<tr>
<td>CLL RTL</td>
<td>7106</td>
<td>1, 4</td>
<td>15</td>
<td>CLEAR LINK - ROTATE TWO LEFT</td>
</tr>
<tr>
<td>CLL RAR</td>
<td>7110</td>
<td>1, 4</td>
<td>15</td>
<td>CLEAR LINK - ROTATE ACCUMULATOR RIGHT</td>
</tr>
<tr>
<td>CLL RTR</td>
<td>7112</td>
<td>1, 4</td>
<td>15</td>
<td>CLEAR LINK - ROTATE TWO RIGHT</td>
</tr>
</tbody>
</table>

Table 2-3

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>LOGICAL SEQUENCE</th>
<th>NUMBER OF STATES</th>
<th>DECIMAL CONSTANT</th>
<th>INSTRUCTIONS COMBINED</th>
</tr>
</thead>
<tbody>
<tr>
<td>NL0000</td>
<td>7300</td>
<td>1</td>
<td>10</td>
<td>0</td>
<td>CLA CLL</td>
</tr>
<tr>
<td>NL0001</td>
<td>7301</td>
<td>1, 3</td>
<td>10</td>
<td>1</td>
<td>CLA CLL IAC</td>
</tr>
<tr>
<td>NL0002</td>
<td>7305</td>
<td>1, 3, 4</td>
<td>15</td>
<td>2</td>
<td>CLA CLL IAC RAL</td>
</tr>
<tr>
<td>NL0003</td>
<td>7325</td>
<td>1, 2, 3, 4</td>
<td>15</td>
<td>3</td>
<td>CLA CLL CML IAC RAL</td>
</tr>
<tr>
<td>NL0004</td>
<td>7307</td>
<td>1, 3, 4</td>
<td>15</td>
<td>4</td>
<td>CLA CLL IAC RTL</td>
</tr>
<tr>
<td>NL0006</td>
<td>7327</td>
<td>1, 2, 3, 4</td>
<td>15</td>
<td>6</td>
<td>CLA CLL CML IAC RTL</td>
</tr>
<tr>
<td>NL0100</td>
<td>7303</td>
<td>1, 3, 4</td>
<td>15</td>
<td>64</td>
<td>CLA CLL CML IAC</td>
</tr>
<tr>
<td>NL2000</td>
<td>7332</td>
<td>1, 2, 4</td>
<td>15</td>
<td>1024</td>
<td>CLA CLL CML RTR</td>
</tr>
<tr>
<td>NL3777</td>
<td>7350</td>
<td>1, 2, 4</td>
<td>15</td>
<td>2047</td>
<td>CLA CLL CMA RAR</td>
</tr>
<tr>
<td>NL4000</td>
<td>7330</td>
<td>1, 2, 4</td>
<td>15</td>
<td>-0</td>
<td>CLA CLL CML RAR</td>
</tr>
<tr>
<td>NL5777</td>
<td>7352</td>
<td>1, 2, 4</td>
<td>15</td>
<td>-1025</td>
<td>CLA CLL CMA RTL</td>
</tr>
<tr>
<td>NL6000</td>
<td>7333</td>
<td>1, 2, 3, 4</td>
<td>15</td>
<td>-1024</td>
<td>CLA CLL CML IAC RTL</td>
</tr>
<tr>
<td>NL7775</td>
<td>7346</td>
<td>1, 2, 4</td>
<td>15</td>
<td>-3</td>
<td>CLA CLL CMA RAL</td>
</tr>
<tr>
<td>NL7776</td>
<td>7344</td>
<td>1, 2, 4</td>
<td>15</td>
<td>-2</td>
<td>CLA CLL CMA RAL</td>
</tr>
<tr>
<td>NL7777</td>
<td>7340</td>
<td>1, 2</td>
<td>10</td>
<td>-1</td>
<td>CLA CLL CMA</td>
</tr>
</tbody>
</table>

Group 2 Microinstructions

Figure 7 shows the instruction format of group 2 microinstructions. Bits 4 - 10 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4 - 7 or 9 - 10 is set, the instruction is a microprogrammed combination group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 7.

Logical Sequences:
1 (BIT 8 = 0) -SMA or SZA or SNL
   (BIT 8 = 1) -SPA or SNA or SZL
2 - CLA
3 - OSR, HLT

* Reverse sensing BIT:
   Unconditional SKIP when BITS 5, 6, & 7 are 0's
   Bits 5, 6, 7 are 0's

Figure 7 – Group 2 Microinstruction Format

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions. Skip microinstructions which have a 0 in bit 8, however, may not be microprogrammed with skip microinstructions which have a 1 in bit 8. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or when bit 8 is 1, the decision will be based on the logical AND.
<table>
<thead>
<tr>
<th>MNE-MONIC</th>
<th>OCTAL CODE</th>
<th>LOGICAL SEQUENCE</th>
<th>NUMBER OF STATES</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td>7400</td>
<td>1</td>
<td>10</td>
<td>NO OPERATION - See Group 1 microinstructions.</td>
</tr>
<tr>
<td>CLA</td>
<td>7600</td>
<td>2</td>
<td>10</td>
<td>CLEAR ACCUMULATOR - The accumulator is loaded with binary O's.</td>
</tr>
<tr>
<td>HLT</td>
<td>7402</td>
<td>3</td>
<td>10</td>
<td>HALT - Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.</td>
</tr>
<tr>
<td>SKP</td>
<td>7410</td>
<td>1</td>
<td>10</td>
<td>SKIP - The content of the PC is incremented by 1, to skip the next instruction.</td>
</tr>
<tr>
<td>SNL</td>
<td>7420</td>
<td>1</td>
<td>10</td>
<td>SKIP ON NON-ZERO LINK - The content of L is sampled; the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.</td>
</tr>
<tr>
<td>SZL</td>
<td>7430</td>
<td>1</td>
<td>10</td>
<td>SKIP ON ZERO LINK - The instruction is skipped if the link contains a 0.</td>
</tr>
<tr>
<td>SZA</td>
<td>7440</td>
<td>1</td>
<td>10</td>
<td>SKIP ON ZERO ACCUMULATOR - The content of the AC is sampled; the next sequential instruction is skipped if all AC bits are 0. If any bit in the AC is a 1, the next instruction is executed.</td>
</tr>
<tr>
<td>SNA</td>
<td>7450</td>
<td>1</td>
<td>10</td>
<td>SKIP ON NON-ZERO ACCUMULATOR - The next instruction is skipped if any one bit of the AC contains a 1. If every bit in the AC is 0, the next instruction is executed.</td>
</tr>
<tr>
<td>SMA</td>
<td>7500</td>
<td>1</td>
<td>10</td>
<td>SKIP ON MINUS ACCUMULATOR - If the content of AC(0) contains a negative two's complement number, the next sequential instruction is skipped. If AC(0) contains a 0, the next instruction is executed.</td>
</tr>
<tr>
<td>SPA</td>
<td>7510</td>
<td>1</td>
<td>10</td>
<td>SKIP ON POSITIVE ACCUMULATOR - If the content of AC(0) contains a 0, indicating a positive two's complement number, the next sequential instruction is skipped.</td>
</tr>
<tr>
<td>OSR</td>
<td>7404</td>
<td>3</td>
<td>15</td>
<td>OR WITH SWITCH REGISTER - The content of the Switch Register is inclusively OR'd with the content of the AC and the result stored in the AC. The HM-6100 sequences the OSR instruction through a 2-cycle execute phase referred to as OPR 2A and OPR 2B. This instruction provides the simplest way to input data to the HM-6100 from peripherals.</td>
</tr>
<tr>
<td>LAS</td>
<td>7604</td>
<td>1, 3</td>
<td>15</td>
<td>LOAD ACCUMULATOR WITH SWITCH REGISTER - The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.</td>
</tr>
</tbody>
</table>
Table 3-2 lists every legal combination of skip microinstructions, along with the resulting condition upon which the decision to skip or execute the next sequential instruction is based. When these combinations include a CLA, the accumulator is cleared after the decision is made. This is a useful trick to save code when a new value will be TAD’ed into the AC.

**TABLE 3-2**

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>LOGICAL SEQUENCE</th>
<th>NUMBER OF STATES</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SZA SNL</td>
<td>7460</td>
<td>1</td>
<td>10</td>
<td>Skip if AC = 0 or L = 1 or both.</td>
</tr>
<tr>
<td>SNA SZL</td>
<td>7470</td>
<td>1</td>
<td>10</td>
<td>Skip if AC ≠ 0 and L = 0.</td>
</tr>
<tr>
<td>SMA SNL</td>
<td>7520</td>
<td>1</td>
<td>10</td>
<td>Skip if AC &lt; 0 or L = 1 or both.</td>
</tr>
<tr>
<td>SPA SZL</td>
<td>7530</td>
<td>1</td>
<td>10</td>
<td>Skip if AC ≥ 0 and L = 0</td>
</tr>
<tr>
<td>SMA SZA</td>
<td>7540</td>
<td>1</td>
<td>10</td>
<td>Skip if AC &lt; 0.</td>
</tr>
<tr>
<td>SPA SNA</td>
<td>7550</td>
<td>1</td>
<td>10</td>
<td>Skip if AC &gt; 0.</td>
</tr>
<tr>
<td>SMA SZA SNL</td>
<td>7560</td>
<td>1</td>
<td>10</td>
<td>Skip if AC &lt; 0 or L = 1 or both.</td>
</tr>
<tr>
<td>SPA SNA SZL</td>
<td>7570</td>
<td>1</td>
<td>10</td>
<td>Skip if AC &gt; 0 and L = 0.</td>
</tr>
</tbody>
</table>

When writing an actual program, it is useful to think in terms of the FORTRAN relational operators – .LT., .EQ., etc. – when trying to compare numbers. The following method along with Table 3-3 will provide this.

**TABLE 3-3**

<table>
<thead>
<tr>
<th>SKIP IF</th>
<th>UNSIGNED COMPARE</th>
<th>SIGNED COMPARE</th>
</tr>
</thead>
<tbody>
<tr>
<td>A .NE. B</td>
<td>SNA</td>
<td>SNA</td>
</tr>
<tr>
<td>A .LT. B</td>
<td>SNL</td>
<td>SNA</td>
</tr>
<tr>
<td>A .LE. B</td>
<td>SNL SZA</td>
<td>SMA SZA</td>
</tr>
<tr>
<td>A .EQ. B</td>
<td>SZA</td>
<td>SZA</td>
</tr>
<tr>
<td>A .GE. B</td>
<td>SL</td>
<td>SPA</td>
</tr>
<tr>
<td>A .GT. B</td>
<td>SIZ SNA</td>
<td>SPA SNA</td>
</tr>
</tbody>
</table>

**GROUP 3 MICROINSTRUCTIONS**

Figure 8 shows the instruction format of group 3 microinstructions which requires bits 3 and 11 to contain a 1. Bits 4, 5 or 7 may be set to indicate a specific group 3 microinstruction. If more than one of the bits is set, the instruction is a microprogrammed combination of group 3 microinstructions following the logical sequence listed in Figure 8.

```
0 1 2 3 4 5 6 7 8 9 10 11
1 1 1 1 CLA MQA * MQL * * * 1
```

Logical Sequences: * Don’t care
1 - CLA
2 - MQA, MQL
3 - NOP

**FIGURE 8 – Group 3 Microinstruction Format**
### TABLE 4

<table>
<thead>
<tr>
<th>MNE-MONIC</th>
<th>OCTAL CODE</th>
<th>LOGICAL SEQUENCE</th>
<th>NUMBER OF STATES</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td>7401</td>
<td>3</td>
<td>10</td>
<td>NO OPERATION - See group 1 microinstructions.</td>
</tr>
<tr>
<td>CLA</td>
<td>7600</td>
<td>1</td>
<td>10</td>
<td>CLEAR ACCUMULATOR</td>
</tr>
<tr>
<td>MQA</td>
<td>7501</td>
<td>2</td>
<td>10</td>
<td>MQ REGISTER INTO ACCUMULATOR - The content of the MQ is logical OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the programmer with an inclusive OR operation.</td>
</tr>
<tr>
<td>MQL</td>
<td>7421</td>
<td>2</td>
<td>10</td>
<td>MQ REGISTER LOAD - The content of the AC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost. This is similar to a DCA instruction.</td>
</tr>
<tr>
<td>ACL</td>
<td>7701</td>
<td>1, 2</td>
<td>10</td>
<td>CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR - This is equivalent to a microprogrammed combination of CLA and MQA. It is similar to the two instruction combination of CLA and TAD.</td>
</tr>
<tr>
<td>CAM</td>
<td>7621</td>
<td>1, 2</td>
<td>10</td>
<td>CLEAR ACCUMULATOR AND MQ REGISTER - The content of the AC and MQ are loaded with binary 0's. This is equivalent to a microprogram combination of CLA and MQL.</td>
</tr>
<tr>
<td>SWP</td>
<td>7521</td>
<td>2</td>
<td>10</td>
<td>SWAP ACCUMULATOR AND MQ REGISTER - The content of the AC and MQ are interchanged by accomplishing a microprogrammed combination of MQA and MQL.</td>
</tr>
<tr>
<td>CLA SWP</td>
<td>7721</td>
<td>1, 2</td>
<td>10</td>
<td>CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER - The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared.</td>
</tr>
</tbody>
</table>

---

**Input Output Transfer Instructions (IOT)**

The input/output transfer instructions, which have an OPCODE of 6G are used to initiate the operation of peripheral devices and to transfer data between peripherals and the HM-6100. Three types of data transfer may be used to receive or transmit information between the HM-6100 and one or more peripheral I/O devices. PROGRAMMED DATA TRANSFER provides a straightforward means of communicating with relatively slow I/O devices, such as Teletypes, cassettes, card readers and CRT displays. INTERRUPT TRANSFERS use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with the data I/O operations. Both Programmed Data Transfers and Program Interrupt Transfers use the accumulator as a buffer, or storage area, for all data transfers. Since data may be transferred only between the accumulator and the peripheral, only one 12 bit word at a time may be transferred. DIRECT MEMORY ACCESS, DMA, Transfers variable-size blocks of data between high-speed peripherals and the memory with minimum of program control required by the HM-6100.

**IOT INSTRUCTION FORMAT**

The Input/Output Transfer instruction format is represented in Figure 9.

```
0 1 2 3 4 5 6 7 8 9 10 11
1 1 0 USER DEFINABLE BITS
```

Basic IOT Instruction: 6XXX8

```
0 1 2 3 4 5 6 7 8 9 10 11
1 1 0 DEVICE SELECTION CONTROL
```

PDP-8/E Format: 6NNX8

**FIGURE 9 — IOT Instruction Format**
The first three bits, 0 - 2, are always set to 68 (110) to specify an IOT instruction. The next 9 bits, 3 - 11, are user definable and can provide a minimal implementation when each bit controls one operation. When following PDP-8/E format, the next six bits, 3 - 8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permit interface with up to 64 I/O devices. The last three bits, 9 - 11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

PROGRAMMED DATA TRANSFER

Programmed Data Transfer is the easiest, simplest, most convenient and most common means of performing data I/O. For microprocessor applications, it may also be the most cost effective approach. The data transfer begins when the HM-6100 fetches an instruction from the memory and recognizes that the current instruction is an IOT. This is referred to as IFETCH and consists of five (5) internal states. The HM-6100 sequences the IOT instruction through a 2-cycle execute phase referred to as IOTA and IOTB. Bits 0 - 11 of the IOT instruction are available on DX0 - 11 at IOTA ^/ LXMAR. These bits must be latched in an external address register. DEVSEL is active low to enable data transfers between the HM-6100 and the peripheral device. Input-Output Instruction Timing is shown in Figure 10. The selected peripheral device communicates with the HM-6100 through 4 control lines - C0, C1, C2 and SKP. In the HM-6100 the type of data transfer, during an IOT instruction, is specified by the peripheral device(s) by asserting the control lines as shown in Tables 5-1 and 5-2.

The control line SKP, when low during an IOT, causes the HM-6100 to skip the next sequential instruction. This feature is used to sense the status of various signals in the device interface. The C0, C1, and C2 lines are treated independently of the SKP line. In the case of a RELATIVE or ABSOLUTE JUMP, the skip operation is performed after the jump. The input signals to the HM-6100, DX0 - 11, C0, C1, C2 and SKP, are sampled during IOTA on the rising edge of time state 3. The data from the HM-6100 is available to the device during DEVSEL ^ XTC. The IOTB cycle is internal to the HM-6100 to perform the operations requested during IOTA. Both IOTA and IOTB consists of six (6) internal states.

![FIGURE 10 - Input-output instruction timing](image)
### TABLE 5-1
**AC DATA TRANSFERS**

<table>
<thead>
<tr>
<th>CONTROL LINES</th>
<th>OPERATION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SKP</td>
<td>C0</td>
<td>C1</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

### TABLE 5-2
**PC VECTOR TRANSFERS**

<table>
<thead>
<tr>
<th>CONTROL LINES</th>
<th>OPERATION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SKP</td>
<td>C0</td>
<td>C1</td>
</tr>
<tr>
<td>H</td>
<td>*</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>*</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>*</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>*</td>
<td>L</td>
</tr>
</tbody>
</table>

* Don't Care

### PROGRAM INTERRUPT TRANSFERS

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced or eliminated altogether. It also provides a means of performing concurrent programmed data transfers between the HM-6100 and the peripheral devices. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device status is set, indicating that the device is actually ready to perform the next data transfer, or that is requires some sort of intervention from the running program.
TABLE 6
PROCESSOR IOT INSTRUCTIONS

<table>
<thead>
<tr>
<th>MNE-MONIC</th>
<th>OCTAL CODE</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SKON</td>
<td>6000</td>
<td>SKIP IF INTERRUPT ON - If Interrupt system is enabled, the next sequential instruction is skipped. The Interrupt system is disabled.</td>
</tr>
<tr>
<td>ION</td>
<td>6001</td>
<td>INTERRUPT TURN ON - The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction.</td>
</tr>
<tr>
<td>IOF</td>
<td>6002</td>
<td>INTERRUPT TURN OFF - The interrupt system is disabled. Note that the interrupt system is automatically disabled when the CPU acknowledges an INT request.</td>
</tr>
<tr>
<td>SRQ</td>
<td>6003</td>
<td>SKIP IF INT REQUEST - The next sequential instruction is skipped if the INT request bus is low.</td>
</tr>
<tr>
<td>GTF</td>
<td>6004</td>
<td>GET FLAGS - The following machines states are read into the indicated bits of AC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>bit 0 - Link</td>
</tr>
<tr>
<td></td>
<td></td>
<td>bit 1 - Greater than flag*</td>
</tr>
<tr>
<td></td>
<td></td>
<td>bit 2 - INT request bus</td>
</tr>
<tr>
<td></td>
<td></td>
<td>bit 3 - Interrupt Inhibit FF*</td>
</tr>
<tr>
<td></td>
<td></td>
<td>bit 4 - Interrupt Enable FF*</td>
</tr>
<tr>
<td></td>
<td></td>
<td>bit 5 - User flag*</td>
</tr>
<tr>
<td></td>
<td></td>
<td>bit 6 - 11 - Save Field Register*</td>
</tr>
<tr>
<td></td>
<td></td>
<td>* These bits are modified by external devices driving the DX bus and the C-lines (C0 = L, C1 = L). For example, bits 1 and 6 - 11 are part of the Extended Memory Control.</td>
</tr>
<tr>
<td>RTF</td>
<td>6005</td>
<td>RETURN FLAGS - Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states. (ex. Extended memory control). (C0 = H, C1 = H)</td>
</tr>
<tr>
<td>SGT</td>
<td>6006</td>
<td>SKIP ON GREATER THAN FLAG - Operation is determined by external devices, if any. This flag is external and must control the skip line.</td>
</tr>
<tr>
<td>CAF</td>
<td>6007</td>
<td>CLEAR ALL FLAGS - AC and link are cleared. Interrupt system is disabled.</td>
</tr>
</tbody>
</table>

The interrupt system allows certain external conditions to interrupt the computer program by driving the INTREQ input to the HM-6100 low. If no higher priority requests are outstanding and the interrupt system is enabled, the HM-6100 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the Interrupt Enable Flip-Flop in the HM-6100 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

The current content of the Program Counter, PC, is deposited in location 0000g of the memory and the program fetches the instruction from location 0001g. The return address is available in location 0000g. This address must be saved, possibly in a software stack, if nested interrupts are permitted. The INTGNT signal is activated by the HM-6100 when a device interrupt is acknowledged. This signal is reset by executing any IOT instruction. The INTGNT is also useful in implementing an External Vectored Priority Interrupt network.

The user program controls the interrupt mechanism of the HM-6100 by executing the processor IOT instructions listed in Table 6. Several of these interrupt IOT instructions are also used if the memory is extended beyond 4K words.

DIRECT MEMORY ACCESS (DMA)

Direct Memory Access, sometimes called data break, is the preferred form of data transfer for use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The HM-6100 is involved only in setting up the transfer; the transfers take place with no processor intervention on a “cycle stealing” basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The device generates a DMA Request when it is ready to transfer data. The HM-6100 grants the DMAREQ by activating the DMAGNT signal at the end of the current instruction. The HM-6100 suspends any further instruction fetches until the DMAREQ line is released. The DX lines are tri-stated, all SEL lines are high, and the external timing signals XTA, XTB, and XTC are active. The device which generated the DMAREQ must provide the address and necessary control signals to the memory for data transfers. The DMAREQ line can also be used as a level sensitive “pause” line.
Control Panel Interrupt Transfer

The HM-6100 CPU provides a unique Control Panel (CP) feature through its CPREQ input and CPSEL output lines. After acknowledging the control panel request, the CPU generates the necessary timing to execute program code in CP memory while also providing the capability to transfer data between CP memory and the user memory using the AC as a buffer. This allows the user memory to be examined and/or modified by the CP software. The CPU will output the MEMSEL signal for all user memory references while the CPSEL signal is generated for CP memory references as shown in Figure 11.

The designer can make use of the control panel features to implement various functions that will be “transparent” to the user’s (main) memory. Some of the more common functions include:

- Binary Loader and Punch
- Register Examination and Modification
- Single Cycle
- Octal Debug with Breakpoints
- Octal listing
- Auto Bootstrap

When a CPREQ is granted the PC is stored in location 0000 of Panel Memory and the HM-6100 resumes operation at location 7777 of the Panel Memory. The CPREQ bypasses the interrupt enable system and the processor IOT instruction, ION and IOF, are ignored while the HM-6100 is in the Control Panel Mode. Once a CPREQ is granted, the HM-6100 will not recognize any DMAREQ or INTREQ until the CPREQ has been fully serviced.

During Control Panel program execution access to the user memory is gained through use of indirect TAD, AND, DCA and ISZ instructions. The CPU will transfer control from CPSEL to MEMSEL during the execute phase of these instructions. The instructions are always fetched from control panel memory.

Exiting from the control panel routine is achieved by executing the following sequence:

- ION
- JMP I 0000 /Exit via location 0000 in Panel Memory

Location 0000 contains either the original return address deposited by the HM-6100 when the CP routine was entered, or it may be a new starting address defined by the CP routine.

Internal Priority Structure

After an instruction is completely sequenced, the major state generator scans the internal priority network as shown in Figure 12. The state of the priority network decides the next sequence of the HM-6100.

The CPU samples the RESET line, the request lines CPREQ, DMAREQ, and INTREQ, and the state of its internal RUN flip-flop during the last execute cycle of each instruction. The worst case response time of the HM-6100 to an external request is, therefore, the time required to execute the longest instruction preceded by any 6-state execution cycle. For the HM-6100, this is an autoindexed ISZ, 22 states, preceded by any 6-state execution cycle instruction. The worst case response time is, therefore, 28 states, 14 µs at 4MHz clock frequency.
When the HM-6100 is initially powered up, the state of the timing generator is undefined. The generator is automatically initialized with a maximum of 34 clock pulses. The request inputs, as the HM-6100 is powered on, must span at least 58 clock pulses to be recognized, 34 clocks for the counter to initialize and a maximum of two HM-6100 cycles (20 to 24 clocks) for the state generator to sample the request lines. A positive transition of RUN/HLT should occur at least 10 clock pulses after RESET to be recognized.

The priority hierarchy is:

- **RESET** - If the RESET line is asserted at the sample time, the processor immediately sets its program counter to 7777, clears the Accumulator and Link, and puts the processor in the HALT state. While halted, the processor continues to cycle and generate the timing signals XTA, XTB, and XTC. During reset the DX line is tristated and the SEL lines are high.

- **CPREQ** - If the RESET line is not found to be asserted, but the CPREQ line is, the processor grants the control panel interrupt request at the end of the current cycle.

- **RUN/HLT** - If neither of the foregoing lines are asserted, but the processor finds its internal RUN FF in the halt state, it enters the HALT cycle at the end of the last execute cycle. Pulsing the RUN/HLT line low causes the HM-6100 to alternately run and halt. The internal RUN FF changes state on the rising edge of the RUN/HLT line. While halted the processor continues to generate the timing signals XTA, XTB, and XTC.

- **DMAREQ** - DMA requests are granted at the end of the current cycle only if none of the above actions are pending.

- **INTREQ** - An interrupt request is granted at the end of the current cycle only if none of the higher priority lines preempt it.

- **IFETCH** - If none of the above actions are indicated, the processor will fetch the next sequential instruction in the next cycle.

---

**FIGURE 12** – Major processor states and number of clock cycles in each state.

---

**Use of Wait Input**

The HM-6100 samples the WAIT line during input-output data transfers. The WAIT line, if active low, controls the transfer duration. If WAIT is active during input transfers (READ), the CPU waits in the T2 state. For an output transfer (WRITE), WAIT controls the time for which the write data is maintained on the DX lines by extending the T6 state. When operating at the max frequency, the internal delay of the HM-6100 causes the falling edge select lines to be past the WAIT setup time for WRITE. The rising edge of the select line for READ can be used to activate WAIT for a WRITE. The wait duration is an integral multiple of the oscillator time period (Figure 13).
USING AN EXTERNAL CRYSTAL

An inexpensive crystal can be used thereby eliminating the need for a clock generator. The crystal operates at parallel resonance, and thus is looks inductive in the circuit. An “AT” cut crystal should be used because it has a low temperature coefficient and can be used over a wide temperature range. The Feedback resistor and shunt capacitance are included internally. The crystal parameters needed are:

- Frequency
- Mod of Resonance – Parallel (anti-resonant)
- Maximum Power level – 1 milliwatt
- Load Capacitance – 32pF
- Series Resistance (max) – 250Ω

For precise frequency determination the effect of the stray circuit capacitance and internal 30pF capacitance must be taken into account.

USING AN EXTERNAL CLOCK GENERATOR

When a system clock is needed, eg. for a baud rate generator for UARTs, the HM-6100 can be externally clocked, thus eliminating the need for separate crystals. The external clock can be connected to the oscillator output pin while grounding oscillator input. This has the effect of over driving the small internal oscillator inverter causing an increase in supply current.

Duty cycle – 50/50

\[ T_{\text{rise}}, T_{\text{fall}} = 20\text{ns} \]
PIN DEFINITIONS

<table>
<thead>
<tr>
<th>PIN</th>
<th>SYMBOL</th>
<th>ACTIVE LEVEL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>H</td>
<td>Supply voltage.</td>
</tr>
<tr>
<td>2</td>
<td>RUN</td>
<td>H</td>
<td>The signal indicates the run state of the CPU and may be used to power down the external circuitry.</td>
</tr>
<tr>
<td>3</td>
<td>DMAGNT</td>
<td>H</td>
<td>Direct Memory Access Grant—DX lines are three-state.</td>
</tr>
<tr>
<td>4</td>
<td>DMAREQ</td>
<td>L</td>
<td>Direct Memory Access Request—DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the DMAREQ line is released.</td>
</tr>
<tr>
<td>5</td>
<td>CPREQ</td>
<td>L</td>
<td>Control Panel Request—a dedicated interrupt which bypasses the normal device interrupt request structure.</td>
</tr>
<tr>
<td>6</td>
<td>RUN/HLT</td>
<td>L</td>
<td>Pulsing the Run/Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN/HLT flip flop.</td>
</tr>
<tr>
<td>7</td>
<td>RESET</td>
<td>L</td>
<td>Clears the AC and loads 7777g into the CPU.</td>
</tr>
<tr>
<td>8</td>
<td>INTREQ</td>
<td>L</td>
<td>Peripheral device interrupt request.</td>
</tr>
<tr>
<td>9</td>
<td>XTA</td>
<td>H</td>
<td>External coded minor cycle timing—signifies input transfers to the HM-6100.</td>
</tr>
<tr>
<td>10</td>
<td>LXMAR</td>
<td>H</td>
<td>The Load External Address Register is used to store memory and peripheral address externally.</td>
</tr>
<tr>
<td>11</td>
<td>WAIT</td>
<td>L</td>
<td>Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as WAIT is active. The CPU is in the lowest power state with clocks running.</td>
</tr>
<tr>
<td>12</td>
<td>XTB</td>
<td>H</td>
<td>External coded minor cycle timing—signifies output transfers from the HM-6100.</td>
</tr>
<tr>
<td>13</td>
<td>XTC</td>
<td>H</td>
<td>External coded minor cycle timing—used in conjunction with the Select Lines to specify read or write operations.</td>
</tr>
<tr>
<td>14</td>
<td>OSC OUT</td>
<td></td>
<td>Crystal input to generate the internal timing (also external clock input).</td>
</tr>
<tr>
<td>15</td>
<td>OSC IN</td>
<td></td>
<td>See Pin 14—OSC OUT (also external clock ground).</td>
</tr>
<tr>
<td>16</td>
<td>DX0</td>
<td></td>
<td>DataX—multiplexed data in, data out and address lines.</td>
</tr>
<tr>
<td>17</td>
<td>DX1</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>18</td>
<td>DX2</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>19</td>
<td>DX3</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>20</td>
<td>DX4</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>21</td>
<td>DX5</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>22</td>
<td>DX6</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>23</td>
<td>DX7</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>24</td>
<td>DX8</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>25</td>
<td>DX9</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>26</td>
<td>GND</td>
<td></td>
<td>Ground.</td>
</tr>
<tr>
<td>27</td>
<td>DX10</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>28</td>
<td>DX11</td>
<td></td>
<td>See Pin 16—DX0.</td>
</tr>
<tr>
<td>29</td>
<td>LINK</td>
<td>H</td>
<td>Link flip flop.</td>
</tr>
<tr>
<td>30</td>
<td>DEVSEL</td>
<td>L</td>
<td>Device Select for I/O transfers.</td>
</tr>
<tr>
<td>31</td>
<td>SWSEL</td>
<td>L</td>
<td>Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a Group 2 Operate Instruction which reads a 12 bit external switch register and OR’s it with the contents of the AC.</td>
</tr>
<tr>
<td>32</td>
<td>00</td>
<td>L</td>
<td>Control line inputs from the peripheral device during an I/O transfer (Table 5).</td>
</tr>
<tr>
<td>33</td>
<td>C1</td>
<td>L</td>
<td>See Pin 32—CO.</td>
</tr>
<tr>
<td>34</td>
<td>C2</td>
<td>L</td>
<td>See Pin 32—CO.</td>
</tr>
<tr>
<td>35</td>
<td>SKP</td>
<td>L</td>
<td>Skips the next sequential instruction if active during an I/O instruction. (Table 5) Instruction Fetch Cycle.</td>
</tr>
<tr>
<td>36</td>
<td>IFETCH</td>
<td>H</td>
<td>Memory Select for memory transfers.</td>
</tr>
<tr>
<td>37</td>
<td>MEMSEL</td>
<td>L</td>
<td>The Control Panel Memory Select becomes active, instead of the MEMSEL, for control panel routines. Signal may be used to distinguish between control panel and main memories.</td>
</tr>
<tr>
<td>38</td>
<td>CPSEL</td>
<td>L</td>
<td>Peripheral device Interrupt Grant Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.</td>
</tr>
<tr>
<td>39</td>
<td>INTGNT</td>
<td>H</td>
<td>Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.</td>
</tr>
<tr>
<td>40</td>
<td>DATAF</td>
<td>H</td>
<td>Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.</td>
</tr>
</tbody>
</table>
Features

- HM-6100 COMPATIBLE
- LOW POWER TYP. < 5.0 μW STANDBY
- SINGLE SUPPLY 4–11 VOLTS
- FULL TEMPERATURE RANGE ~55°C TO +125°C
- STATIC OPERATION
- 4 PROGRAMMABLE OUTPUTS (FLAGS)
- 4 PROGRAMMABLE SENSE INPUTS
- CONTROL FOR TWO 12-BIT INPUT PORTS
- CONTROL FOR TWO 12-BIT OUTPUT PORTS
- PRIORITY VECTORED INTERRUPTS
- UP TO 31 PIE'S PER SYSTEM
- 16 INSTRUCTIONS FOR PIE CONTROL

Description

The HD-6101 Parallel Interface Elements (PIE) are high speed, low power, silicon gate CMOS general purpose devices which provide addressing interrupt and control for a variety of peripheral functions, such as UARTs, FIFOs, Keyboards, etc. Data transfers between the HM-6100 CMOS Microprocessor and the HD-6101 are via Input-Output Transfer (IOT) instructions, control lines and DX bus.

Data transfers between peripheral devices and the DX bus are controlled by the PIE via 2 read, 2 write, 4 sense and 4 flag functions. Internal PIE registers are programmed under software control for write polarities, sense levels or edges, flag values and interrupt enables. Another software controlled register stores the address for vectored interrupt operation.

Functional Diagram

---

2-24
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+12.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V to VCC +0.3V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6101A-9</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military HD-6101A-2</td>
<td>-55°C to +125°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Electrical Characteristics

**VCC = 10.0 ±0.5 Volts; TA = Industrial or Military**

### D.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70%</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td></td>
<td>20%</td>
<td>V</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage(1)</td>
<td>VCC</td>
<td>-2.0</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td></td>
<td>0.45</td>
<td>V</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current (Static)</td>
<td>1.0</td>
<td>800</td>
<td>μA</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance(2)</td>
<td>5</td>
<td>7</td>
<td>pF</td>
</tr>
<tr>
<td>C0</td>
<td>Output Capacitance(2)</td>
<td>8</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>CIO</td>
<td>Input/Output Capacitance(2)</td>
<td>8</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

### Notes:

1. Except pins 33, 34, 39
2. Guaranteed and sampled, but not 100% tested.

### A.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>tDR</td>
<td>Delay: DEVSEL to READ</td>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>150</td>
<td>165 ns</td>
</tr>
<tr>
<td>tDW</td>
<td>Delay: DEVSEL to WRITE</td>
<td>50</td>
<td>110</td>
<td>50</td>
<td>150</td>
<td>165 ns</td>
<td></td>
</tr>
<tr>
<td>tDF</td>
<td>Delay: DEVSEL to FLAG</td>
<td>100</td>
<td>200</td>
<td>50</td>
<td>150</td>
<td>165 ns</td>
<td></td>
</tr>
<tr>
<td>tDC</td>
<td>Delay: DEVSEL to CI, C2</td>
<td>105</td>
<td>215</td>
<td>220</td>
<td>220</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDI</td>
<td>Delay: DEVSEL to SRP/INT</td>
<td>105</td>
<td>215</td>
<td>240</td>
<td>240</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDA</td>
<td>Delay: DEVSEL to DX</td>
<td>175</td>
<td>215</td>
<td>240</td>
<td>240</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tLX</td>
<td>LXMAR Pulse Width</td>
<td>100</td>
<td>120</td>
<td>135</td>
<td>135</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tAS</td>
<td>Address Set-Up Time</td>
<td>30</td>
<td>40</td>
<td>45</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tAH</td>
<td>Address Hold Time</td>
<td>50</td>
<td>50</td>
<td>55</td>
<td>55</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDS</td>
<td>Data Set-Up Time</td>
<td>40</td>
<td>65</td>
<td>70</td>
<td>70</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>50</td>
<td>50</td>
<td>55</td>
<td>55</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

### Notes:

1. All devices guaranteed at worst case limits. Room temperature, 10V data provided for information — not guaranteed.
Specifications HD-6101

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+8.0V</td>
<td>VCC</td>
<td>VCC</td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V</td>
<td>+0.3V</td>
<td>VCC</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td>-65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>Industrial HD-6101-9</td>
<td>-40°C to +85°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Military HD-6101-2</td>
<td>-55°C to +125°C</td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

VCC = 5.0V ±10%; TA = Industrial or Military

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical “1” Input Voltage</td>
<td>70% VCC</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logical “0” Input Voltage</td>
<td>20% VCC</td>
<td>V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td>μA</td>
<td></td>
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</tr>
<tr>
<td>VOH</td>
<td>Logical “1” Output Voltage</td>
<td>2.4</td>
<td>V</td>
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<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Logical “0” Output Voltage</td>
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<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current (Static)</td>
<td>1.0</td>
<td>100</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance(2)</td>
<td>5</td>
<td>7</td>
<td>µF</td>
<td></td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance(2)</td>
<td>8</td>
<td>10</td>
<td>µF</td>
<td></td>
</tr>
<tr>
<td>CIO</td>
<td>Input/Output Capacitance(2)</td>
<td>8</td>
<td>10</td>
<td>µF</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: (1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>tDR</td>
<td>Delay: DEVSEL to READ</td>
<td>200</td>
<td>300</td>
<td>330</td>
<td>ns</td>
<td>CL = 50pF</td>
<td></td>
</tr>
<tr>
<td>tDW</td>
<td>Delay: DEVSEL to WRITE</td>
<td>100</td>
<td>220</td>
<td>140</td>
<td>300</td>
<td>330</td>
<td>ns</td>
</tr>
<tr>
<td>tDF</td>
<td>Delay: DEVSEL to FLAG</td>
<td>200</td>
<td>375</td>
<td>415</td>
<td>ns</td>
<td></td>
<td>Diagram</td>
</tr>
<tr>
<td>tDC</td>
<td>Delay: DEVSEL to C1, C2</td>
<td>160</td>
<td>460</td>
<td>510</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDI</td>
<td>Delay: DEVSEL to SKP/INT</td>
<td>210</td>
<td>460</td>
<td>510</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDA</td>
<td>Delay: DEVSEL to DX</td>
<td>350</td>
<td>460</td>
<td>510</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tLX</td>
<td>LXMAR Pulse Width</td>
<td>200</td>
<td>240</td>
<td>265</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tAS</td>
<td>Address Set-Up Time</td>
<td>60</td>
<td>80</td>
<td>90</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tAH</td>
<td>Address Hold Time</td>
<td>100</td>
<td>125</td>
<td>140</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDS</td>
<td>Data Set-Up Time</td>
<td>50</td>
<td>80</td>
<td>80</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>100</td>
<td>100</td>
<td>110</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.
Specifications HD-6101C-9

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+8.0V</td>
<td>+8.0V</td>
<td>+8.0V</td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V to VCC +0.3V</td>
<td>GND -0.3V to VCC +0.3V</td>
<td>GND -0.3V to VCC +0.3V</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td>-65°C to +150°C</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>Industrial HD-6101C-9</td>
<td>-40°C to +85°C</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

VCC = 5.0V ±5%; TA = Industrial

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td>.8V</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>.1V</td>
<td>.1V</td>
<td>V</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-10 μA</td>
<td>+10 μA</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage(1)</td>
<td>2.4V</td>
<td>0.45V</td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>-10 μA</td>
<td>+10 μA</td>
<td>V</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>1,0 μA</td>
<td>1,0 μA</td>
<td>V</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current (Static)</td>
<td>5 μA</td>
<td>800 μA</td>
<td>V</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance(2)</td>
<td>5 pF</td>
<td>7 pF</td>
<td>pF</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance(2)</td>
<td>8 pF</td>
<td>10 pF</td>
<td>pF</td>
</tr>
<tr>
<td>CIO</td>
<td>Input/Output Capacitance(2)</td>
<td>8 pF</td>
<td>10 pF</td>
<td>pF</td>
</tr>
</tbody>
</table>

NOTES:
(1) Except pins 33, 34, 39
(2) Guaranteed and sampled, but not 100% tested.

TA = 25°C VCC = 5.0V(1) TA = INDUSTRIAL VCC = 5V ±5%

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>tDR</td>
<td>Delay: DEVSEL to READ</td>
<td>230 ns</td>
<td>375 ns</td>
<td>230 ns</td>
<td>375 ns</td>
<td>ns</td>
<td>CL = 50pF</td>
</tr>
<tr>
<td>tDW</td>
<td>Delay: DEVSEL to WRITE</td>
<td>100 ns</td>
<td>240 ns</td>
<td>125 ns</td>
<td>375 ns</td>
<td>ns</td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tDF</td>
<td>Delay: DEVSEL to FLAG</td>
<td>230 ns</td>
<td>475 ns</td>
<td>230 ns</td>
<td>475 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDC</td>
<td>Delay: DEVSEL to C1, C2</td>
<td>190 ns</td>
<td>560 ns</td>
<td>190 ns</td>
<td>560 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDI</td>
<td>Delay: DEVSEL to SKP/INT</td>
<td>250 ns</td>
<td>560 ns</td>
<td>250 ns</td>
<td>560 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDA</td>
<td>Delay: DEVSEL to DX</td>
<td>400 ns</td>
<td>560 ns</td>
<td>400 ns</td>
<td>560 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tLX</td>
<td>LXMAR Pulse Width</td>
<td>230 ns</td>
<td>300 ns</td>
<td>230 ns</td>
<td>300 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tAS</td>
<td>Address Set-Up Time</td>
<td>80 ns</td>
<td>100 ns</td>
<td>80 ns</td>
<td>100 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tAH</td>
<td>Address Hold Time</td>
<td>120 ns</td>
<td>150 ns</td>
<td>120 ns</td>
<td>150 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDS</td>
<td>Data Set-Up Time</td>
<td>60 ns</td>
<td>90 ns</td>
<td>60 ns</td>
<td>90 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>120 ns</td>
<td>150 ns</td>
<td>120 ns</td>
<td>150 ns</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

NOTE (1): All devices guaranteed at worst case limits. Room temperature, 5V data provided for information – not guaranteed.
Timing for a typical transfer is shown below. During an instruction fetch the processor places the contents of the PC on the bus \( 1 \) and obtains from memory an IOT instruction of the form 6XXX \( 2 \). During IOTA of the execute phase the processor places that instruction back on the DX lines \( 3 \) and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on DEVSEL while XTC is high \( 4 \) is used by the addressed PIE along with the decoded control information to generate CPU control signals \( C_1, C_2 \), and \( \text{SKP} \). Also at this time either the Control Register A or the Interrupt Vector Register are outputed on the DX lines, or control outputs \( \text{READ1} \) and \( \text{READ2} \) are generated to gate peripheral data to the DX lines. A low going pulse on DEVSEL while XTC is low \( 5 \) is used to generate WRITE 1 and WRITE 2 controls. These signals are used to latch accumulator data into peripheral devices.

All PIE timing is generated from HM-6100 signals LXMAR, DEVSEL, and XTC. No additional timing signals, clocks, or one shots are required.

Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the HM-6100.
The HM-6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the pin programmable select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIEs. Address zero is reserved for IOT's internal to the HM-6100. The four control bits are decoded by the PIE to select one of 16 instructions which are described below.

### PIE Address and Instructions

#### PIE Instruction Format

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>CONTROL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1 0</td>
<td></td>
</tr>
</tbody>
</table>

#### Control Mnemonics and Action

<table>
<thead>
<tr>
<th>CONTROL</th>
<th>MNEMONICS</th>
<th>ACTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>READ1</td>
<td>The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate onto the DX bus to be “OR'ed” with the HM-6100 accumulator data. The HM-6100 accumulator is cleared prior to reading peripheral data when CO is asserted low.</td>
</tr>
<tr>
<td>1000</td>
<td>READ2</td>
<td></td>
</tr>
<tr>
<td>0001</td>
<td>WRITE1</td>
<td>The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the HM-6100 accumulator data on the DX lines into peripheral data registers. The HM-6100 AC is cleared after the write operation when the CO input is asserted low.</td>
</tr>
<tr>
<td>1001</td>
<td>WRITE2</td>
<td></td>
</tr>
<tr>
<td>0010</td>
<td>SKIP1</td>
<td>The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the SKP/INT output causing the HM-6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE does not assert the SKP/INT output and the HM-6100 will execute the next instruction.</td>
</tr>
<tr>
<td>0011</td>
<td>SKIP2</td>
<td></td>
</tr>
<tr>
<td>1010</td>
<td>SKIP3</td>
<td></td>
</tr>
<tr>
<td>1011</td>
<td>SKIP4</td>
<td></td>
</tr>
<tr>
<td>0110</td>
<td>RCRA</td>
<td>The Read Control Register A instruction gates the contents of CRA onto the DX lines during time 3 to be “OR” transferred to the HM-6100 AC.</td>
</tr>
<tr>
<td>0101</td>
<td>WCRA</td>
<td>The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer HM-6100 AC data on the DX lines during time 5 of IOTA into the appropriate register.</td>
</tr>
<tr>
<td>1101</td>
<td>WCRB</td>
<td></td>
</tr>
<tr>
<td>1100</td>
<td>WVR</td>
<td></td>
</tr>
<tr>
<td>0100</td>
<td>SFLAG1</td>
<td>The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs SFLAG1 and SFLAG3 follow the data stored in bits FL1 and FL3 of CRA.</td>
</tr>
<tr>
<td>1110</td>
<td>SFLAG3</td>
<td></td>
</tr>
<tr>
<td>0111</td>
<td>CFLAG1</td>
<td>The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.</td>
</tr>
<tr>
<td>1111</td>
<td>CFLAG3</td>
<td></td>
</tr>
<tr>
<td>(6007)B</td>
<td>CAF</td>
<td>HM-6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops.</td>
</tr>
</tbody>
</table>

#### Programmable Outputs

**FLAGS (1-4)** - The FLAGS are general purpose outputs that can be set and cleared under program control. FLAG1 follows bit FL1 in Control Register A and etc. FLAGS can be changed by loading new data into CRA via the WCRA commands. In addition, FLAG1 and FLAG3 can be set and cleared directly by the commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
Programmable Sense Inputs

The sense inputs are used to set sense flip flops (SENSE FF) inside the PIE. For each sense input there are two FF's, one for skip and one for interrupt. Conditions for setting each SENSE FF, levels or edges and positive or negative polarities, are set by control bits SL and SP in CRB.

The SENSE FF’s are sampled when LXMAR is high. Interrupt requests are generated only when the sense flip flops are set by an edge and interrupts are enabled by writing to control reg A. Sense flip flops are reset on the following conditions.

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>SENSE FLIP FLOPS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SKIP FF</td>
</tr>
<tr>
<td>CAF Instruction (60078)</td>
<td>Clears All</td>
</tr>
<tr>
<td>SKIP Instruction</td>
<td>Clears Corresponding FF</td>
</tr>
<tr>
<td>Vectored Interrupt</td>
<td>Not Cleared</td>
</tr>
<tr>
<td>Interrupt Disabled (IE = &quot;0&quot;)</td>
<td>Not Cleared</td>
</tr>
</tbody>
</table>

Controls for Input and Output Ports

READ (1-2) — The READ outputs are activated by the read instructions and are used by peripheral devices to get data onto the DX lines for transfer to the HM-6100. Read lines are active low.

WRITE (1-2) — The WRITE outputs are activated by the write instructions and are used by peripheral devices to load HM-6100 AC data from the DX lines into peripheral data registers. Output polarity is controlled by the WRITE POLARITY bits of CRA. A logic one causes pulses to be positive while a logic zero causes pulses to be negative.

I/O CONTROL LINES — There are three I/O control lines from the PIE to the microprocessor — CI, C2, and INT/SKP. The type of data transfer, during an IOT instruction, is specified by the PIE's assertion of the CI and C2 control lines as shown below.

Interrupt and skip information are time multiplexed on the same line (SKP/INT). Since the HM-6100 samples the sense flip flops and generates an interrupt request for enabled bits (IE1-4) when LXMAR is high. Interrupt requests are asserted by the PIE driving the INT/SKP line low. During IOTA of SKIP instructions the INT/SKP reflects the SENSE FF data when DEVSEL is low and XTC is high. If the SENSE flip flop is set, the INT/SKP line is driven low to cause the HM-6100 to skip the next instruction. All these outputs are open drain.

<table>
<thead>
<tr>
<th>CONTROL LINES</th>
<th>OPERATION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>SKP</td>
<td>C0*</td>
<td>CI</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

NOTE: *The C0 line must be connected to VCC using a pull-up resistor.
Programmable Registers

CONTROL REGISTER A (CRA)

The CRA can be read and written by the HM-6100 via the RCRA and WCRA commands.

The format and meaning of control bits are shown below.

FL (1-4) — Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits under software control changes the corresponding FLAG outputs.

IE (1-4) — A high level on INTERRUPT ENABLE enables interrupts for the SENSE inputs.

Otherwise these inputs provide conditional skip testing as defined by the SKIP1-4 instructions.

WP (1-2) — A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs.

CONTROL REGISTER B (CRB)

The CRB can be written by the HM-6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown.

SL (1-4) — A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level in the SL bits causes the SENSE inputs to be edge sensitive. An interrupt request is generated only if a sense line is set up to be edge sensitive and interrupts are enabled via the IE bits of CRA.

SP (1-4) — A high level on the SENSE POLARITY bits causes the flip flop to be set by high level or positive going edge. A low level causes the flip flop to be set by a low level or negative going edge.

VECTOR REGISTER

A hardware priority network uniquely selects a PIE to provide a vectored address. The first IOT command of any type, after the HM-6100 signal INTERRUPT GRANT goes high, resets the INTGNT line to a low level. The INTGNT signal is used to freeze the priority network and enable vector generation. The highest priority PIE has PIN tied to VCC. The lowest priority PIE is the last one on the chain. Within the PIE, SENSE1 has the highest priority and SENSE 4 has the lowest. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt. If PIN is tied to GND, then the PIE will respond as a non-vectored interrupt device.
## Pin Definitions

<table>
<thead>
<tr>
<th>PIN</th>
<th>SYMBOL</th>
<th>ACTIVE LEVEL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>H</td>
<td>Positive voltage</td>
</tr>
<tr>
<td>2</td>
<td>INTGNT</td>
<td>H</td>
<td>A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.</td>
</tr>
<tr>
<td>3</td>
<td>PRIN</td>
<td>H</td>
<td>A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.</td>
</tr>
<tr>
<td>4</td>
<td>SENSE 4</td>
<td>PROG</td>
<td>The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the sense flip flop to be set by a level while a low SL level causes the sense flip flop to be set by an edge. A high SP level will cause the sense flip flop to be set by a positive going edge or high level. A high IC (interrupt enable) level generates an interrupt request whenever the sense flip flop is set by an edge.</td>
</tr>
<tr>
<td>5</td>
<td>SENSE 3</td>
<td>PROG</td>
<td>See pin 4 – SENSE 4</td>
</tr>
<tr>
<td>6</td>
<td>SENSE 2</td>
<td>PROG</td>
<td>See pin 4 – SENSE 4</td>
</tr>
<tr>
<td>7</td>
<td>SENSE 1</td>
<td>PROG</td>
<td>See pin 4 – SENSE 4</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PIN</th>
<th>SYMBOL</th>
<th>ACTIVE LEVEL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>SEL 3</td>
<td>TRUE</td>
<td>Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.</td>
</tr>
<tr>
<td>9</td>
<td>SEL 4</td>
<td>TRUE</td>
<td>See Pin 8 – SEL 3</td>
</tr>
<tr>
<td>10</td>
<td>LXMAR</td>
<td>H</td>
<td>A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(13-11) into the address register.</td>
</tr>
<tr>
<td>11</td>
<td>SEL 5</td>
<td>TRUE</td>
<td>See Pin 8 – SEL 3</td>
</tr>
<tr>
<td>12</td>
<td>SEL 6</td>
<td>TRUE</td>
<td>See Pin 8 – SEL 3</td>
</tr>
<tr>
<td>13</td>
<td>XTC</td>
<td>H</td>
<td>The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on DEVSEL initiates a &quot;read&quot; operation. When XTC is low, a low going pulse on DEVSEL initiates a write operation.</td>
</tr>
<tr>
<td>14</td>
<td>SEL 7</td>
<td>TRUE</td>
<td>See Pin 8 – SEL 3</td>
</tr>
<tr>
<td>15</td>
<td>DX 0</td>
<td>TRUE</td>
<td>Data transfers between the microprocessor and PIE take place via these input/output pins.</td>
</tr>
<tr>
<td>16</td>
<td>DX 1</td>
<td>TRUE</td>
<td>See Pin 15 – DX 0</td>
</tr>
<tr>
<td>17</td>
<td>DX 2</td>
<td>TRUE</td>
<td>See Pin 15 – DX 0</td>
</tr>
<tr>
<td>18</td>
<td>DX 3</td>
<td>TRUE</td>
<td>See Pin 15 – DX 0</td>
</tr>
<tr>
<td>19</td>
<td>DX 4</td>
<td>TRUE</td>
<td>See Pin 15 – DX 0</td>
</tr>
<tr>
<td>20</td>
<td>DX 5</td>
<td>TRUE</td>
<td>See Pin 15 – DX 0</td>
</tr>
</tbody>
</table>

## Diagram

![HD-6101 Diagram](image-url)
HARRIS HD-6102
SEMICONDUCTOR PRODUCTS DIVISION

MEMORY EXTENSION/DMA/INTERVAL TIMER/CONTROLLER
(MEDIC)

Features

• HM-6100 COMPATIBLE
• LOW POWER – TYP. < 5.0µW STANDBY
• SINGLE SUPPLY 4 – 11 VOLTS
• FULL TEMPERATURE RANGE -55°C TO +125°C
• STATIC OPERATION
• SINGLE PHASE CLOCK, ON CHIP CRYSTAL OSC.
• SOFTWARE COMPATIBLE WITH PDP-8/E
• PROVIDES ADDRESSING UP TO 32 WORDS
• PROVIDES SIMULTANEOUS DMA
• DMA CHANNEL CAN BE USED FOR DYNAMIC RAM
• 12-BIT PROGRAMMABLE INTERVAL TIMER
• HARDWARE RESET
• PRIORITY VECTORED INTERRUPTS
• 28 DIFFERENT I/O INSTRUCTIONS

Description

The HD-6102 is a multi-function peripheral controller circuit incorporating such functions as memory extension, direct memory access control, and a programmable real time clock.

The HD-6102 provides the necessary control to address up to 32K words of memory, and its DMA channel can be used with Dynamic RAM Components for “transparent refresh”. The programmable real time clock is 12-bits long, and its output frequency can be programmed for 5 decades.

It features a high degree of system integration, putting into one chip all the functions which are normally available in three or more LSI circuits. As a result of this large integration, the user can design and produce a compact microcomputer with minicomputer performance.

Pinout

<table>
<thead>
<tr>
<th>Pin</th>
<th>Description</th>
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<tbody>
<tr>
<td>1</td>
<td>VCC</td>
</tr>
<tr>
<td>2</td>
<td>DMAEN</td>
</tr>
<tr>
<td>3</td>
<td>DMAINT</td>
</tr>
<tr>
<td>4</td>
<td>MEMSEL</td>
</tr>
<tr>
<td>5</td>
<td>IFETCH</td>
</tr>
<tr>
<td>6</td>
<td>MEMSEL*</td>
</tr>
<tr>
<td>7</td>
<td>RESET</td>
</tr>
<tr>
<td>8</td>
<td>UP</td>
</tr>
<tr>
<td>9</td>
<td>XTA</td>
</tr>
<tr>
<td>10</td>
<td>LXMAR</td>
</tr>
<tr>
<td>11</td>
<td>LXMAR*</td>
</tr>
<tr>
<td>12</td>
<td>XTC*</td>
</tr>
<tr>
<td>13</td>
<td>XTC</td>
</tr>
<tr>
<td>14</td>
<td>CLOCK</td>
</tr>
<tr>
<td>15</td>
<td>SKP/INT</td>
</tr>
<tr>
<td>16</td>
<td>DX0</td>
</tr>
<tr>
<td>17</td>
<td>DX1</td>
</tr>
<tr>
<td>18</td>
<td>DX2</td>
</tr>
<tr>
<td>19</td>
<td>DX3</td>
</tr>
<tr>
<td>20</td>
<td>DX4</td>
</tr>
<tr>
<td>21</td>
<td>GND</td>
</tr>
</tbody>
</table>

Functional Diagram
Specifications HD-6102A

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+12.0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V to VCC +0.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HO-6102A-9</td>
<td>-55°C to +125°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military HO-6102A-2</td>
<td></td>
<td></td>
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<td></td>
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**ELECTRICAL CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIHC</td>
<td>Logical &quot;1&quot; Osc. Input Voltage</td>
<td>VCC - 5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>-0.3 V</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VILC</td>
<td>Logical &quot;0&quot; Osc. Input Voltage</td>
<td>GND + 5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>1.0</td>
<td>1.0</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>VCC -2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V0L</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>0.45</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>ICC1</td>
<td>Supply Current (Static)</td>
<td>900</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>ICC2</td>
<td>Supply Current (Operating) (HO-6102A-9)</td>
<td>4.0</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>ICC2</td>
<td>Supply Current (Operating) (HO-6102A-2)</td>
<td>4.0</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance (4)</td>
<td>7</td>
<td>8</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance (4)</td>
<td>8</td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CIO</td>
<td>Input/Output Capacitance (4)</td>
<td>8</td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>COSC</td>
<td>Oscillator IN/OUT Capacitance (4)</td>
<td>30</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTES:**
2. Except pins 31, 32, 33, 34.
4. Guaranteed and sampled, but not 100% tested.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIHC</td>
<td>Logical &quot;1&quot; Osc. Input Voltage</td>
<td>VCC - 5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>-0.3 V</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VILC</td>
<td>Logical &quot;0&quot; Osc. Input Voltage</td>
<td>GND + 5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>1.0</td>
<td>1.0</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>VCC -2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V0L</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>0.45</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>ICC1</td>
<td>Supply Current (Static)</td>
<td>900</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>ICC2</td>
<td>Supply Current (Operating) (HO-6102A-9)</td>
<td>4.0</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>ICC2</td>
<td>Supply Current (Operating) (HO-6102A-2)</td>
<td>4.0</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance (4)</td>
<td>7</td>
<td>8</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance (4)</td>
<td>8</td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CIO</td>
<td>Input/Output Capacitance (4)</td>
<td>8</td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>COSC</td>
<td>Oscillator IN/OUT Capacitance (4)</td>
<td>30</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

**TEST CONDITIONS**

- **TA = 25°C**
  - VCC = 10V
  - Fc = 5.5MHz
- **TA = INDUSTRIAL 10 ±0.5V, Fc = 5.7MHz**
- **TA = MILITARY 10 ±0.5V, Fc = 5.0MHz**

**NOTE 1:** All devices guaranteed at worst case limits. Room temperature, 10V data provided for information – not guaranteed.

---

2-34
## Specifications HD-6102

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>70% VCC</td>
<td>VCC - 5 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>20% VCC</td>
<td>GND + 5 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-1.0 μA</td>
<td>1.0 μA</td>
<td>0V ≤ VIN ≤ VCC</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>2.4</td>
<td>V</td>
<td>10H = 0.2mA</td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6102-9</td>
<td>45</td>
<td>V</td>
<td>IO L = 2.0mA</td>
<td></td>
</tr>
<tr>
<td>Military HD-6102-2</td>
<td>800</td>
<td>mA</td>
<td>VCC = 5.0V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2.0</td>
<td>mA</td>
<td>VCC = 5.0V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>500</td>
<td>ns</td>
<td>VCC = 5.0V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>120</td>
<td>ns</td>
<td>Freq. = 3.33MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>120</td>
<td>ns</td>
<td>Freq. = 2.5MHz</td>
<td></td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS

**VCC = 5.0 ±10% Volts**  **TA = Industrial or Military**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Unit</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical ’1’ Input Voltage</td>
<td></td>
<td>70% VCC</td>
<td>VCC - 5 V</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical ’0’ Input Voltage</td>
<td></td>
<td>20% VCC</td>
<td>GND + 5 V</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>μA</td>
<td>-1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical ’1’ Output Voltage</td>
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<td>45 V</td>
<td>0.45 V</td>
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<tr>
<td>VOL</td>
<td>Logical ’0’ Output Voltage</td>
<td></td>
<td>45 V</td>
<td>0.45 V</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>μA</td>
<td>-1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>ICC1</td>
<td>Supply Current (Static)</td>
<td>μA</td>
<td>800</td>
<td>2.0</td>
</tr>
<tr>
<td>ICC2</td>
<td>Supply Current (Operating)</td>
<td>μA</td>
<td>2.0</td>
<td>0V ≤ VO ≤ VCC</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>pF</td>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance</td>
<td>pF</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>COI</td>
<td>Input/Output Capacitance</td>
<td>pF</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>COSC</td>
<td>Oscillator IN OUT Capacitance</td>
<td>pF</td>
<td>30</td>
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</table>

### TEST CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>LXMAR *Pulse Width</td>
<td>250</td>
<td>300</td>
<td>ns</td>
<td>CL = 50pF</td>
</tr>
<tr>
<td>Address Set-Up Time</td>
<td>70</td>
<td>80</td>
<td>ns</td>
<td>See Timing</td>
</tr>
<tr>
<td>Address Hold Time</td>
<td>100</td>
<td>120</td>
<td>ns</td>
<td>Diagram</td>
</tr>
<tr>
<td>Delay: DEVSEL to DX</td>
<td>350</td>
<td>400</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Delay: DEVSEL to CT</td>
<td>350</td>
<td>400</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Delay: DEVSEL to SKP/INT</td>
<td>350</td>
<td>400</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Data Input Set-Up Time</td>
<td>100</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Data Input Hold Time</td>
<td>100</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>RESET Input Pulse Width</td>
<td>500</td>
<td>600</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Delay: SKP/INT to SKP/INT</td>
<td>120</td>
<td>130</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Delay: XTC to XTC*, MEMSEL to MEMSEL*, LXMAR to LXMAR*</td>
<td>120</td>
<td>130</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Enable/Disable Time: DMAGNT to EMA Lines</td>
<td>80</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>MEMSEL* Pulse Width READ</td>
<td>550</td>
<td>750</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>MEMSEL* Pulse Width WRITE</td>
<td>700</td>
<td>950</td>
<td>ns</td>
<td></td>
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<td>MEMSEL* Pulse Width WRITE</td>
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<td>550</td>
<td>ns</td>
<td></td>
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<tr>
<td>LXMAR *Pulse Width</td>
<td>260</td>
<td>350</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA READ Access Time: LXMAR to UP</td>
<td>85</td>
<td>750</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA READ Access Time: LXMAR to UP</td>
<td>85</td>
<td>750</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA READ Access Time: LXMAR to UP</td>
<td>85</td>
<td>750</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA READ Access Time: LXMAR to UP</td>
<td>85</td>
<td>750</td>
<td>ns</td>
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<tr>
<td>DMA READ Access Time: LXMAR to UP</td>
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<td>750</td>
<td>ns</td>
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<tr>
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<td>85</td>
<td>750</td>
<td>ns</td>
<td></td>
</tr>
<tr>
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<td>85</td>
<td>750</td>
<td>ns</td>
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</tr>
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<td>750</td>
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<td>DMA READ Access Time: LXMAR to UP</td>
<td>85</td>
<td>750</td>
<td>ns</td>
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</tr>
<tr>
<td>MEMSEL* Pulse Width WRITE</td>
<td>400</td>
<td>550</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA WRITE Access Time: LXMAR* to MEMSEL*</td>
<td>550</td>
<td>750</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA WRITE Access Time: LXMAR* to MEMSEL*</td>
<td>550</td>
<td>750</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA WRITE Access Time: LXMAR* to MEMSEL*</td>
<td>550</td>
<td>750</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA WRITE Access Time: LXMAR* to MEMSEL*</td>
<td>550</td>
<td>750</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>MEMSEL* Pulse Width WRITE</td>
<td>800</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DMA WRITE Access Time: LXMAR* to MEMSEL*</td>
<td>100</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA WRITE Access Time: LXMAR* to MEMSEL*</td>
<td>100</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA WRITE Access Time: LXMAR* to MEMSEL*</td>
<td>100</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA WRITE Access Time: LXMAR* to MEMSEL*</td>
<td>100</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>DMA WRITE Access Time: LXMAR* to MEMSEL*</td>
<td>100</td>
<td>100</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Up Pulse Width DMA WRITE</td>
<td>400</td>
<td>550</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Up Pulse Width DMA WRITE</td>
<td>400</td>
<td>550</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Up Pulse Width DMA WRITE</td>
<td>400</td>
<td>550</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Up Pulse Width DMA WRITE</td>
<td>400</td>
<td>550</td>
<td>ns</td>
<td></td>
</tr>
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</table>

**NOTE:** All devices guaranteed at worst case limits. Room temperature, 5V data provided for information — not guaranteed.
Specifications HD-6102C-9

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+8.0V</td>
<td>-0.3V to VCC +0.3V</td>
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<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-40°C to +85°C</td>
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</tr>
<tr>
<td>Operating Temperature Range</td>
<td>Industrial HD-6102C-9</td>
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</tbody>
</table>

### ELECTRICAL CHARACTERISTICS

VCC = 5.0 ±5% Volts  TA = Industrial

#### D.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td>V</td>
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<tr>
<td>VIHC</td>
<td>Logical &quot;1&quot; Osc. Input Voltage</td>
<td>VCC -5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VILC</td>
<td>Logical &quot;0&quot; Osc. Input Voltage</td>
<td>GND +5</td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage(1)</td>
<td>2.4</td>
<td>V</td>
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<td></td>
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<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage(2)</td>
<td>+10</td>
<td>μA</td>
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<td></td>
</tr>
<tr>
<td>IO</td>
<td>Input Leakage</td>
<td>-10</td>
<td>μA</td>
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<tr>
<td>ICC1</td>
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<td>mA</td>
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<tr>
<td>ICC2</td>
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<td>mA</td>
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<td>Input Capacitance(4)</td>
<td>7</td>
<td>pF</td>
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<td>CO</td>
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<td>8</td>
<td>pF</td>
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<tr>
<td>CIG</td>
<td>Input/Output Capacitance(4)</td>
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<td>pF</td>
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<td>COSC</td>
<td>Oscillator IN/OUT Capacitance(4)</td>
<td>30</td>
<td>pF</td>
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#### A.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
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<th>UNITS</th>
<th>TEST CONDITIONS</th>
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<tbody>
<tr>
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<td>LXMAR Pulse Width IN</td>
<td>300</td>
<td>ns</td>
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<tr>
<td>tAIS</td>
<td>Address Set-Up Time IN</td>
<td>80</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>tAITH</td>
<td>Address Hold Time IN</td>
<td>120</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>tDA</td>
<td>Delay DEVSEL to DX</td>
<td>400</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDC</td>
<td>Delay DEVSEL to CT, C2</td>
<td>400</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDI</td>
<td>Delay DEVSEL to SKP/INT</td>
<td>400</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>tDIS</td>
<td>Data Input Set-Up Time</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>tDIH</td>
<td>Data Input Hold Time</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
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<td>tRST</td>
<td>RESET Input Pulse Width</td>
<td>500</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tSID</td>
<td>Delay SKP/INTX to SKP/INT</td>
<td>150</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDMLX</td>
<td>Delay XTC to XTC, MEMSEL to MEMSEL*, LXMAR to LXMAR*</td>
<td>150</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>tDEM</td>
<td>Enable/Disable Time: DMAGNT to EMA Lines</td>
<td>100</td>
<td>ns</td>
<td></td>
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<td>tMDR</td>
<td>MEMSEL* Pulse Width READ</td>
<td>750</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>tMDW</td>
<td>MEMSEL* Pulse Width WRITE</td>
<td>950</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>tMDWR</td>
<td>MEMSEL* Pulse Width WRITE/REFRESH</td>
<td>550</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tLD</td>
<td>LXMAR* Pulse Width</td>
<td>350</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDRAT</td>
<td>DMA READ Access Time: LXMAR to UP</td>
<td>750</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDXAS</td>
<td>DX &amp; EMA Address Setup</td>
<td>120</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDXAH</td>
<td>DX &amp; EMA Address Hold</td>
<td>175</td>
<td>ns</td>
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<tr>
<td>tDREN</td>
<td>DMA READ Enable Time: MEMSEL* to UP</td>
<td>750</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tRUP</td>
<td>UP Pulse Width DMA READ</td>
<td>550</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDWAT</td>
<td>DMA WRITE Access Time: LXMAR* to MEMSEL*</td>
<td>350</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDWE</td>
<td>DMA WRITE Enable Time: UP to MEMSEL*</td>
<td>750</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tMWS</td>
<td>MEMSEL* Setup Time DMA Write: MEMSEL* to LXMAR*</td>
<td>550</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDMS</td>
<td>DMAEN Setup Time Write</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDMH</td>
<td>DMAEN Hold Time Write</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tUP</td>
<td>UP Pulse Width DMA WRITE</td>
<td>750</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. All devices guaranteed at worst case limits. Room temperature, 5V data provided for information – not guaranteed.
Timing Diagrams

FIGURE 1-1 - DMA Read

FIGURE 1-2 - DMA Read/Refresh

FIGURE 1-3 - DMA Write

FIGURE 1-4 - DMA Write/Refresh
**HD-6102 System Timing**

The three-state bi-directional 12-bit DX bus is used to transfer data and control information between the HD-6102 and the HM-6100 microprocessor. The HM-6100 transmits the device address and control information on the DX bus during the 'execute' phase of an Input-Output Transfer (IOT) instruction. The HD-6102 accepts this information on the falling edge of the LXMAR (Address Latch Enable) Signal.

The device selection bits (3-8) are compared within the HD-6102 and if these are 00, 13, or 2X, the MEDIC decodes the control bits (9-11) for execution. DEVSEL goes low, during the first half of an IOT execute machine cycle for a read operation and it goes low again in the second half for a write operation.

The HD-6102 responds to a 'read' instruction by putting data on the DX bus when DEVSEL is low. During the write operation, the MEDIC accepts data from the HM-6100 Accumulator on the rising edge of the DEVSEL.

SKP/INT line goes low during the 'read' DEVSEL if the HD-6102 is responding to a 'skip' instruction, and the 'skip' condition is met, therefore causing the HM-6100 to skip the next sequential instruction. SKP/INT line reflects the interrupt request status of the HM-6100 at all times except during the 'read' DEVSEL. The SKP/INT line goes low if an active interrupt request is pending. During read DEVSEL mode, the SKP/INT indicates the current skip condition.

---

**Architecture**

The HD-6102 is composed of three distinct functions:

(A) A DMA port that uses the bus during the second half of a cycle to read, write, or refresh memory. The DMA port logic includes a word count register WC, a current address register CA, an extended current address register ECA, and a DMA status register.

(B) An extended memory address controller that augments the 12-bit addresses generated by the HM-6100 microprocessor by supplying a 3-bit address field that may be decoded to select one of eight 4096 word memory fields. The memory extension controller logic consists of an instruction field register IF, a data field register DF, an instruction buffer register IB, and a save field register SF.

(C) A realtime clock whose mode and time base rate may be programmed by the user. The clock logic includes a clock enable register CE, a clock buffer register CB, a clock counter register CC, and a time base multiplexer.
A. Simultaneous DMA Channel

The SDMA registers are summarized as follows:

**CURRENT ADDRESS (CA) REGISTER**

This register is a 12-bit presettable binary counter. At the beginning of a SDMA transfer, the current address must be set to the first location to be accessed. The content of the CA register is incremented by 1 after a SDMA transfer, and the incremented value is used as the address of the memory location with which the next transfer will be performed.

**EXTENDED CURRENT ADDRESS (ECA) REGISTER**

This is a 3-bit presettable binary counter and if the carry enable bit of the DMA status register is set, the 12-bit CA register and the 3 ECA bits are treated as one 15-bit register with the ECA bits most significant. If memory field 7 (all 3 bits at logic one) is selected, the ECA cannot increment, but will wrap around in field 7 and an F7 error (F7E) will occur. The Interrupt Enable bit IE in SR11 must be set to enable F7E interrupts. If enabled, the F7E will request an interrupt. If the carry enable bit CE in SR9 is not set, the ECA is not incremented when CA goes from 7777g to 0000g.

**WORD COUNT (WC) REGISTER**

A 12-bit presettable binary counter is used as a word counter. At the beginning of a SDMA transfer, the two's complement of the number of 12-bit words to be transferred must be loaded into the WC. If enabled, this will initiate the SDMA operation. The WC register is incremented by 1 after a SDMA transfer. If this value becomes zero, word count overflow has occurred and if the IE bit in SR11 is set, interrupts are enabled and an interrupt is requested. Unless instructed to be in the continuous run mode, a WC overflow inhibits further transfers. The WOF is set when the MSB of the WC register makes a "1" to "0" transition.

**DMA STATUS REGISTER**

This register consists of 5 control bits and 2 flag bits for the SDMA feature. For a description, refer to the register bit assignments.

![Figure 3 - MEDIC Timing for DCA I](Image)
TABLE 1 – SDMA Instructions

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCAR</td>
<td>6205g</td>
<td>LOAD CURRENT ADDRESS REGISTER (CA). Description: The contents of the AC replace the contents of the CA and the AC is cleared. DMA sequencing is stopped.</td>
</tr>
<tr>
<td>RCAR</td>
<td>6215g</td>
<td>READ CURRENT ADDRESS REGISTER. Description: Contents of CA and DMA operation started.</td>
</tr>
<tr>
<td>LWCR</td>
<td>6225g</td>
<td>LOAD WORD COUNT REGISTER (WC). Description: Contents of AC is cleared. DMA operation started.</td>
</tr>
<tr>
<td>LEAR</td>
<td>62N6g</td>
<td>LOAD IMMEDIATE TO EXTENDED CURRENT ADDRESS REGISTER (ECA). Description: Field N of the IOT Instruction is transferred to the Extended current address register.</td>
</tr>
<tr>
<td>REAR</td>
<td>6235g</td>
<td>READ EXTENDED CA. Description: Extended Current Address register contents OR’d into bits 6, 7, 8, of AC.</td>
</tr>
<tr>
<td>LSFR</td>
<td>6245g</td>
<td>LOAD DMA FLAGS and STATUS REGISTER. Description: AC bits 7-11 are transferred to the DMA STATUS REGISTER and the AC is cleared.</td>
</tr>
<tr>
<td>RFSR</td>
<td>6255g</td>
<td>READ DMA FLAGS and STATUS REGISTER. Description: DMA Flags and Status Register bits are OR transferred into AC bits 5-11 and Field 7 wraparound error (F7E) is cleared.</td>
</tr>
<tr>
<td>SKOF</td>
<td>6265g</td>
<td>SKIP ON OVERFLOW INTERRUPT. Description: The PC is incremented by 1 if a Word Count register overflow interrupt condition is present causing next instruction to be skipped.</td>
</tr>
<tr>
<td>WVWR</td>
<td>6275g</td>
<td>WRITE VECTOR REGISTER. Description: AC bits 0-10 are transferred to the Vector Register and the AC is cleared.</td>
</tr>
<tr>
<td>CAF</td>
<td>6007g</td>
<td>CLEAR ALL FLAGS. Description: Clears F7E and WOF (and also COF), clock enable and clock buffer. The DMA process is initiated if the Status Register is not set to the “stop” mode.</td>
</tr>
</tbody>
</table>
TABLE 2 – DMA Flags and Status Register

<table>
<thead>
<tr>
<th>Bit Assignments</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
</tr>
<tr>
<td>*</td>
</tr>
</tbody>
</table>

where* – don’t care for write and zero for read.

F7E    Field 7 wrap around carry error; Cleared by CAF, RFSR and RESET.
WOF    Logic one indicates word counter overflow; clear by CAF, LWCR and RESET.
CE     Carry enable from CA (0–11) to ECA; cleared by RESET.
R/W    Logic one indicates DMA write (Port to Memory transfer). Cleared (DMA Read) by RESET.
SR7, 8 Refresh mode; WC is frozen no UP, DMAEN is don’t care.
00    Normal mode; DMAEN (H) freezes WC, CA and no UP if WC has not overflowed; Stop if WC overflows.
01    Burst mode; DMAEN (H) freezes WC, CA and no UP if WC has not overflowed; refresh condition if WC overflows.
10    Stops DMA.

OPERATION

The HD-6102 SDMA channel augments the throughput of the HM-6100 during DMA operations by transferring data between memory and peripheral devices simultaneously with normal processor bus usage. In other words, no memory cycles are “stolen” from the processor; but the DMA address and data are transferred on the bus during periods that the DX bus is inactive.

DMA MODES

SR7 = SR8 = 0 REFRESH MODE

This is the mode to which the 6102 reverts on RESET. The word count register clock input is disabled, the user pulse (DMA data strobe) is suppressed and the DMAEN input is ignored. However, provided valid DMA transfer conditions are met in a particular memory cycle, the DMA sequencer will be started, appropriate timing signals will be generated and the current address register will be clocked. Thus DMA read accesses will be performed continually with an essentially free-running current address register. Read accesses will refresh dynamic memory. No WOF is possible but an F7E is possible if bit SR9 is set, enabling a carry from the current address register to the extended current address register.

SR7 = 0; SR8F = 1 NORMAL MODE

This mode is used for normal SDMA operations with static memory. The following instruction sequence can be used:

- CLA /Clear AC
- TAD CA /Get starting address
- LCAR /Load into current address register and clear AC
- TAD SR /Get value for DMA status register
- LFSR /Change status (from refresh to normal for example)
- TAD WC /Get two’s complement of block length
- LWCR /Load word count register and start DMA transfers

Note that LWCR will start the sequencer so it should be the last instruction in the initialization sequence. The ECA register and vector register could also have been initialized in this sequence.

The SDMA sequencer samples DMAEN on the rising edge of every XTA and latches the condition of the enable line. If DMAEN is low, the sequencer is enabled, external timing signals XTC*, MEMSEL*, UP, LXMAR* are generated, the WC and CA registers are clocked. If DMAEN is high, at XTA (↑) time, the signal is sampled and latched and if the WC has not overflowed, the WC and CA registers are frozen, UP is suppressed. If the WOF condition comes up, the SDMA operation stops, regardless of DMAEN level.

The DMAEN and UP signals provide a simple interlocked handshaking method for transferring data one or more characters at a time (entire blocks) concurrently with processor operations on the bus. Of course, at all times, independent of DMAEN, the SDMA sequencer can proceed only if other bus usage conditions for DMA operations are met (not IOTA, IAUTOI, DCA, JMS, IJMS, ISZ, DMAGNT, or access of location X0000g).

NOTE: IAUTOI is an indirect cycle of any autoindexed instruction; IJMS is indirect cycle of JMS. An autoindexed JMP instruction may not be executed when the DMA mode is active.

SR7 = 1; SR8 = 1 BURST MODE

This mode is the same as the normal mode except when the word count register overflows. When this happens, the SDMA sequencer will set the WOF flag and revert to the refresh mode (ignoring DMAEN, freezing WC and suppressing UP). This mode is used when SDMA operations and dynamic memory refresh must be concurrently performed. The system designer must control the block lengths to be transferred, the refresh interval, and memory system design according to the application and performance desired.

SR7 = 1; SR8 = 1 STOP MODE

In this mode, no SDMA operations will take place. Naturally, cycle stealing DMA is still possible, and indeed may be used in any of the modes but the designer must be aware that cycle stealing may adversely affect dynamic memory refresh intervals. LWCR and LFSR may be executed in either order to change mode and start DMA.
B. Extended Memory Address Control

The EMA function of the HD-6102 is program compatible with the DEC PDP-8/E KM8-E Memory Extension option. The purpose of the EMA function is to extend the effective addressing space of the system from 4K to 32K words. To perform this function, the EXTENDED MEMORY CONTROLLER maintains a 3-bit extended address which is decoded by the memory modules to select 1 of 8 memory fields each containing 4096 words of storage. These 4K fields start with FIELD 0 and progress to FIELD 7 when 32K of memory is used. All software communication with the controller is via programmed IOT instructions.

The figure below shows two 3-bit field registers: the Instruction Field, which acts as an extension to the Instruction and directly obtained operand addresses and the Data Field, which augments indirectly obtained operand addresses. The program can, therefore, use one field for instructions and address pointers and another field for data. The selection between Instruction and Data Fields is signalled by the DATAF signal generated by the HM-6100. A discussion of the various registers follows.

![EMA Registers](image)

FIGURE 5 — EMA Registers

INSTRUCTION FIELD REGISTER (IF)

The IF is a 3-bit register that serves as an extension to the Program Counter (PC). The IF, however, is not incremented when the PC goes from 7777 to 0000. The contents of the IF determine the field from which all instructions are taken. Operands for all directly addressed memory reference instructions also come from the Instruction Field. The indirect pointer for all indirectly addressed memory reference instructions reside in the Instruction Field. The IF is cleared to 0g and the HM-6100 Program Counter is set to 7777g by RESET.

DATA FIELD REGISTER (DF)

The DF is a 3-bit register which determines the memory field from which operands are fetched in indirectly addressed AND, TAD, ISZ, or DCA instructions. However, the branch address for indirectly addressed JMS or JMP instructions is obtained from the Instruction Field. The Data Field register may be modified under program control. The DF is set to 0g on reset.

INSTRUCTION BUFFER REGISTER (IB)

The IB is a 3-bit register which serves as an input buffer for the Instruction Field (IF) register. All programmed modifications of the IF register are made through the IB register. The transfer from IB to IF takes place at the beginning of the execute phase of the “next” JMP or JMS instruction or immediately upon execution of an IF instruction. Using this feature, a program segment can execute an instruction to modify the IF and “exit” the program segment before the actual modification of the IF takes place. If instructions could change the IF directly, it would be impossible to execute the “next” sequential instruction, followed by a Change IF instruction. The IB to IF transfer is inhibited if the JMP/JMS instruction is fetched from control panel memory, which is restricted to 4K, but the LIF instruction is used here to provide the ability to load the IF register from the IB register. This allows the control panel routines to be executed transparently while the IF and IB differ and also yields a method for the panel to extract or alter the status of the primary EMA registers. The IB is set to 0g, on reset. The IB to IF transfer takes place during the second cycle of a JMP/JMS instruction when XTC makes a falling (↓) transition.

SAVE FIELD REGISTER (SF)

The SF is a 6-bit register in which the IB and DF registers are saved during an Interrupt Grant. When an Interrupt occurs, the contents of IB and DF are automatically stored in SF (0-2) and SF (3-5), respectively, and the IF, IB and DF registers are cleared. The INTGNT (Interrupt Grant) cycle stores the “current” Program Counter (PC) in location 0000g of Memory Field 0g and the CPU resumes operation in location 0001g of Memory Field 0g. The Instruction Field and Data Field of the program segment being executed by the CPU before the interrupt was acknowledged are available in the SF register.

INTERRUPT INHIBIT FLIP-FLOP

The INTREQ (Interrupt Request) line to the HM-6100 must be “gated” by the Interrupt Inhibit Flip-Flop so that, when the Instruction Field is changed under program control, all interrupts are disabled until a JMP, JMS or LIF instruction is executed. Since the actual modification of the Instruction Field takes place only after the “next” JMP/JMS/LIF, this inhibition of the INTREQ’s ensures that the program sequence resumes operation in the “new” memory field before an Interrupt Request is granted.

Since Interrupt Requests are asynchronous in nature, a situation may arise in which an INTREQ is generated when the IF and IB bits are different. The Interrupt Inhibit FF guarantees the structural integrity of the program segment. The IF is cleared on reset.
## TABLE 3 – EMA Instructions

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTF</td>
<td>60048</td>
<td>GET FLAGS</td>
</tr>
</tbody>
</table>
|          |            | Operation: AC (0) ←→ LINK  
|          |            |          | AC (2) ←→ INTREQ Line  
|          |            |          | AC (3) ←→ INT INHIBIT FF  
|          |            |          | AC (4) ←→ INT ENABLE FF  
|          |            |          | AC (6-11) ←→ SF (0-5)  
|          |            | Description: LINK, INTREQ and INT ENABLE FF are internal to the CPU. The INT INHIBIT FF and SF are in the MEDIC. |
| RTF      | 60058      | RETURN FLAGS |
|          |            | Operation: LINK ←→ AC (0)  
|          |            |          | IB ←→ AC (6-8)  
|          |            |          | DF ←→ AC (9-11)  
|          |            | Description: LINK is restored. All AC bits are available externally during T6 of IOTA to restore other flag bits. The Internal Interrupt System is enabled. However, the Interrupt Inhibit FF is set until the "next" JMS/JMP/LIF. The IB is transferred to IF after the "next" JMS/JMP/LIF. |
| CDF      | 62N18      | CHANGE DATA FIELD |
|          |            | Operation: DF ←→ N8  
|          |            | Description: Change DF register to N (0g-7g). |
| CIF      | 62N28      | CHANGE INSTRUCTION FIELD |
|          |            | Operation: IB ←→ N8  
|          |            | Description: Change IB to N (0g-7g). Transfer IB to IF after the "next" JMP/JMS/LIF. The Interrupt Inhibit FF is set until the "next" JMP/JMS/LIF. |
| CDF, CIF | 62N38      | CHANGE DF, IF |
|          |            | Operation: DF ←→ N8  
|          |            |          | IB ←→ N8  
|          |            | Description: Combination of CDF and CIF. |
| RDF      | 62148      | READ DATA FIELD |
|          |            | Operation: AC (6-8) ←→ AC (6-8) + DF  
|          |            | Description: OR's the contents of DF into bits 6-8 of the AC. All other bits are unaffected. |
| RIF      | 62248      | READ INSTRUCTION FIELD |
|          |            | Operation: AC (6-8) ←→ AC (6-8) + IF  
|          |            | Description: OR's the contents of IF into bits 6-8 of the AC. All other bits of the AC are unaffected. |
| RIB      | 62348      | READ INTERRUPT BUFFER  
|          |            | READ SAVE FIELD |
|          |            | Operation: AC (6-22) ←→ AC (6-11) + SF  
|          |            | Description: OR's the contents of SF into bits 6-11 of the AC. All other bits are unaffected. |
| RMF      | 62448      | RESTORE MEMORY FIELD |
|          |            | Operation: IB ←→ SF (0-2)  
|          |            |          | DF ←→ SF (3-5)  
|          |            | Description: The SF register saves the contents of the IB and DF when an interrupt occurs. This command is used to restore IB and DF when "exiting" from the interrupt service routing in another field. Transfer IB to IF after the next JMP/JMS/LIF. The Interrupt Inhibit Flip-Flop is set until the next JMP/JMS/LIF. |
| LIF      | 62548      | LOAD INSTRUCTION FIELD |
|          |            | Operation: IF ←→ IB  
|          |            | Description: Transfer IB to IF and clear the Interrupt Inhibit FF. |

+ "OR"  
^ "AND"  
→ "IS REPLACED BY"
OPERAND FETCHING

Instructions are accessed from the currently assigned Instruction Field. For indirect AND, TAD, ISZ or DCA instructions, the operand address refers first to the Instruction Field to obtain an Effective Address which in turn refers to a location in the currently addressed Data Field. All instructions and operands are obtained from the field designated by the IF, except for indirectly addressed operands, which are specified by the DF. Thus, DF is active only in the Execute phase of an AND, TAD, ISZ or DCA when it is directly preceded by an Indirect phase.

<table>
<thead>
<tr>
<th>ADDRESS MODE</th>
<th>IF</th>
<th>DF</th>
<th>AND, TAD, ISZ or DCA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct</td>
<td>m</td>
<td>n</td>
<td>Operand in field m.</td>
</tr>
<tr>
<td>Indirect</td>
<td>m</td>
<td>n</td>
<td>Absolute address of operand in field m; operand in field n.</td>
</tr>
</tbody>
</table>

Each field of extended memory contains eight auto-index registers in addresses 10 through 17. For example, assume that a program in field 2 is running (IF = 2) and using operands in field 1 (DF = 1) when the instruction TAD 1 10 is fetched. The indirect auto-index cycle is entered, and the contents of location 10 in field 2 are read, incremented, and rewritten. If address 10 in field 2 originally contained 0546, it now contains 0547. In the execute cycle, the operand is fetched from location 0547 of field 1.

Program control is transferred between memory fields by the CIF instruction. The instruction does not change the instruction field directly, as this would make it impossible to execute the next sequential instruction; instead, it loads the new instruction field in the IB for automatic transfer into the IF when either a JMP or JMS instruction is executed. The DF is unaffected by the JMP and JMS instructions.

The 12-bit program counter is set in the normal manner and, because the IF is an extension on the most significant end of the PC, the program sequence resumes in the new memory field following a JMP or JMS. Entry into a program interrupt is inhibited after the CIF instruction until a JMP or JMS is executed.

NOTE: The IF is not incremented if the PC goes from 7777g to 0000g. This feature protects the user from accidentally entering a nonexistent field.

To call a subroutine that is out of the current field, the data field register is set to indicate the field of the calling JMS, which establishes the location of the operands as well as the identity of the return field. The instruction field is set to the field of the starting address of the subroutine. The following sequence returns program control to the main program from a subroutine that is out of the current field.

```
SUBRP, SUBR /POINTER

CIF 10 /CHANGE TO INSTRUCTION
/FIELD 1 = 6212
JMS I SUBRP /SUBRP = ENTRY ADDRESS
```

When a program interrupt occurs, the current instruction and data field numbers are automatically stored in the 6-bit save field register, then the IF and DF are cleared. The 12-bit program counter is stored in location 0000g of field 0g and program control advances to location 0001g of field 0g. At the end of the program interrupt subroutine, the RMF instruction restores the IF and DF from the contents of the SF. Alternatively, the GTF and RTF instructions may be used to handle the Save Field and Link information. The following instruction sequence at the end of the program interrupt subroutine continues the interrupted program after the interrupt has been processed.

```
RETURN, CIF /USE TO FORM CIF N
/INSTRUCTION

CL A /RESTORE AC
TAD AC /READ DATA FIELD INTO AC
RMF /LOAD IB AND DF FROM SF
ION /TURN ON INTERRUPT
/SYSTEM
JMP I 0 /RESTORE PC WITH
/CONTENTS OF LOCATION
/0000g AND LOAD
/IF FROM IB
```

HM-6100 control panel memory programs, if used must be careful in the manner that EMA register data is manipulated. Control panel interrupt requests bypass the device interrupt enable flip flop, and indeed, are granted even by a halted CPU. The interrupts from a control panel may occur at any time, and in particular when the IB and IF registers do not contain the same data. The EMA logic inhibits IB to IF transfers in control panel memory so that panel routines may execute transparently (in particular, JMP/JMS instructions). The panel routines may alter the IF by executing the LIF instructions.

Users should also note that the GTF and RIB instructions read the SF register, and only the RIF instruction reads the IF register. Note also that the SF saves the IB register rather than the IF during an interrupt. However, interrupts are inhibited until the IF and IB registers are the same.

The memory extension controller that we have discussed
in this section shows three important design considerations involved in extending memory addressing space. The first is the concept of having separate instructions and data fields for program flexibility. The second is the importance of double buffering the instruction field register to maintain structural integrity of programs and the third is the provision for saving the current field status upon interrupts and disabling interrupts until a change of instruction field has been completely executed.

### C. Programmable Real Time Clock

The programmable real time clock offers the HM-6102 user a number of ways to accurately measure and count intervals in order to implement real time data acquisition and data processing systems. It is similar in functionality to the DEC PDP-8/E DKB-EP Programmable Real Time Clock option.

The crystal used should have the following characteristics:
- RS ≤ 150 ohms
- CM = 3-30mF (10-15F)
- CO = 10-15pF

Static capacitance should be around 5pF; for the greatest stability, CO should be around 12pF and the oscillator is parallel resonant.

**TABLE 4 – Clock Enable Register Bit Assignments**

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN0</td>
<td>EN2</td>
<td>EN3</td>
<td>EN4</td>
<td>EN5</td>
<td>EN6</td>
<td>EN7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Don’t care for write and zero for read.

Where EN0 When set to 1, enables clock overflow (COF flag) to cause an interrupt. Cleared by RESET, CAF.

EN2 When reset to a 0-counter runs at selected rate. Overflow occurs every 4096 (2^12) counts. COF flag remains set until cleared by either IOT 6135 (CLSA), or CAF, or RESET.

When set to a 1-counter runs at selected rate. If the COF flag is cleared, overflow causes clock buffer to be transferred to the clock counter which continues to run. COF flag remains set until cleared with IOT 6135 (CLSA). Also cleared by RESET, CAF.

EN3, 4, 5 Assuming a 2MHz crystal oscillator cleared by RESET, CAF.

<table>
<thead>
<tr>
<th>EN3</th>
<th>EN4</th>
<th>EN5</th>
<th>Octal</th>
<th>Interval Between Pulses</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Stop</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Stop</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2</td>
<td>200μsec</td>
<td>50Hz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>3</td>
<td>2msec</td>
<td>500Hz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>200μsec</td>
<td>5kHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>5</td>
<td>2μsec</td>
<td>50kHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>6</td>
<td>2μsec</td>
<td>500kHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>7</td>
<td>Stop</td>
<td>0</td>
</tr>
</tbody>
</table>

EN7 Inhibits clock prescaler when set to 1; cleared by RESET or CAF. EN3-5 and EN7 should not be changed simultaneously.

A discussion of the Real Time Clock registers as shown in Figure 6 follows:

**FIGURE 6 – RTC Registers**

**CLOCK ENABLE REGISTER**

This register controls the mode of counting, whether clock interrupts are allowed, and the rate of the time base of the clock. For a description, refer to the register bit assignment.

**CLOCK BUFFER REGISTER (CB)**

This 12-bit register stores data being transferred from the AC to the clock counter, or from the clock counter to the AC. It also permits presetting of the clock counter.

**CLOCK COUNTER REGISTER (CC)**

This register is a 12-bit binary counter that may load the clock buffer or be loaded from it. It is driven by a 2MHz crystal oscillator with the proper predivision set by the time base selection. When an overflow occurs and if bit 0 of the clock enable register is a logic one, an interrupt is requested. If bit 2 is also 1, overflow causes the clock buffer to be transferred automatically into the clock counter.

**TIME BASE MULTIPLEXER**

The multiplexer provides count pulses to the clock counter according to the rate set by the clock enable register. Use of other than a 2MHz crystal for the clock will result in proportionately different time bases.

**CLOCK OVERFLOW FLAG**

This flag is set by a clock counter overflow. It is cleared by CAF, CLSA and RESET. Its complement provides LSB (VR11) of interrupt vector. If EN0 of clock enable counter is set, COF can cause an interrupt request. The COF is set when the MSB of the counter makes a "1" to "0" transition.
TABLE 5 – RTC Instructions

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>OPERATION</th>
</tr>
</thead>
</table>
| CLZE     | 6130g      | CLEAR ENABLE REGISTER PER AC  
Description: Clears the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed. |
| CLSK     | 6131g      | SKIP ON CLOCK INTERRUPT  
Description: Causes the program counter to be incremented by one if clock interrupt conditions exists, so that the next sequential instruction is skipped. |
| CLOE     | 6132g      | SET ENABLE REGISTER PER AC  
Description: Sets the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed. |
| CLAB     | 6133g      | TRANSFER AC TO CLOCK BUFFER  
Description: Causes the contents of the AC to be transferred to the Clock Buffer, then causes the contents of the Clock Buffer to be transferred to the Clock Counter. The AC is not changed. |
| CLEN     | 6134g      | READ CLOCK ENABLE REGISTER  
Description: Causes contents of the Clock Enable Register to be transferred into the AC. |
| CLSA     | 6135g      | READ CLOCK STATUS  
Description: Interrogates the clock overflow status flip flop by clearing AC, then transferring clock status into AC bit 0. COF is cleared. |
| CLBA     | 6136g      | READ CLOCK BUFFER  
Description: Clears the AC, then transfers the contents of the Clock Buffer into the AC. |
| CLCA     | 6137g      | READ CLOCK COUNTER  
Description: Clears the AC, transfers the contents of the Clock Counter to the Clock Buffer, then transfers the contents of the Clock Buffer into the AC. If EN7 is set to 1 (clock prescaler is inhibited), the CLCA instruction increments the prescaler input by one. If the clock is in the "stop" mode but EN7 is not inhibited, the prescaler will not be clocked by the CLCA instruction. |
| CAF      | 6007g      | CLEAR ALL FLAGS  
Description: Clears COF flag (and also F7E, WOF flags), clock enable and clock buffer registers. |

System Considerations

The HD-6102 is the highest priority device in a priority interrupt scheme. It provides an active low signal on pin 40, POUT, to signal the next lower priority device in the chain (thus, a high level on POUT indicates that the 6102 is not requesting an interrupt) via its “priority-in”, PRIN, input.

The HD-6102 when requesting an interrupt activates the SKP/INT line low on pin 35 and the POUT line low on pin 40 if its interrupt inhibit flip-flop is not set.

The IOT instructions used by the HD-6102 preclude the use of certain device addresses when the system uses HD-6101 PIES. The addresses that may not be used are those given by bits 3 through 7 of the IOT instructions that are used with the HD-6102. These addresses are 00101, 01000, 01001, 01010, 01101 corresponding to IOT instructions 612X, 613X, 620X, 621X, 622X, 623X, 624X, 625X, 626X and 627X.

The HD-6102 does not generate DMAREQ signals to the 6100 because of its simultaneous use of the DX bus. It monitors the DMAGNT signal in order to place the EMAO, 1, 2 lines on pins 36, 37, 38 in a high impedance state while DMAGNT is high.

If the application requires other peripherals requiring direct memory access on a cycle stealing basis, for example, bus contention problems will be resolved by the HD-6102 as it monitors the DMAGNT line and gets off the bus (by placing all lines in the high impedance state) when DMAGNT is active.

If interrupts are enabled and a request is pending, during the first INTGNT cycle, the HD-6102 will detect the referencing of location 0000g by the HM-6100 in order to save the PC and will suspend simultaneous DMA during that cycle. The logic will in fact suspend simultaneous DMA in any cycle that location 0000g is referenced, either in main memory or control panel memory.

This makes it possible to disable automatic interrupt vectoring by grounding the INTGNT line to the HD-6102. This will not affect the generation of INTREQ so the HM-6100 will have to poll peripheral devices (skip on flag instructions) to determine the interrupting source.

Grounding INTGNT is not possible in extended memory applications since the INTGNT signal is used to save the Instruction Buffer and Data Field Register and clear the IF, IB and DF registers. (All peripheral device interrupt service routines have their entry point at location 0001g of Memory Field 0g.)
If no interrupt requests are pending in the 6102 (COF, F7E or WOF) from the DMA or RTC functions, the HD-6102 interrupt request flip-flop is clear and POUT, the priority out signal, is high, enabling interrupt requests downstream in the priority chain. In the event that interrupts are enabled (DMA status bit SR1 is set and/or clock enable bit EN0 is set) and an interrupting condition occurs (F7E, WOF, COF), the POUT signal goes low asynchronously disabling interrupt vectors downstream.

If the Interrupt Inhibit Flip-Flop is not set, the SKP/INT line is driven low by the interrupt request. If the IIFF is set, the SKP/INT line stays high until the IIFF is cleared (by RESET or an IB to IF transfer) at which time SKP/INT may be driven low. Skip requests will always propagate independently of IIFF during IOTA \& DEVSEL \& XTC.

Interrupt request from devices downstream of the HD-6102 must also be channeled via the HD-6102 in order that the IIFF may condition the request timing. The HD-6102 provides a built in pull-up on the SKP/INTX line coming in from devices downstream in the priority chain. At 5V, the pull-up looks like a 10K resistor; at 10V, it looks like 5K.

The execution of any IOT instruction will reset INTGNT to a low level at the end of IOTA time. This IOT instruction will be the first instruction in the interrupt service routine after saving status. If hardware vectoring is being used, any IOT instruction when INTGNT is high will cause the HD-6102 to place a vector address on the bus if it requested an interrupt and pull the C1 and C2 lines low, thus placing the vector in PC and forcing a branch to the service routine. If the C2 line is left unconnected, the vector address will not be forced into the PC, but will be OR’ed into the AC. The interrupt service routine would have to execute a CLA after its first IOT instruction in order to clear the AC. Note that the LSB of the vector address is determined by the complement of the COF flag and that a DMA interrupt service routine must distinguish between the two possible interrupting conditions, a word count overflow or a field 7 wrap-around error. The programmer may read the DMA status register with an RFSR instruction and also test the WOF flag with a skip instruction, SKOF. The COF flag may also be tested with the CLSK skip instruction. The flag may be read (and cleared) with the CLSA instruction. The skip instructions cause the SKP/INT line to go low during IOTA \& XTC time if the flag being tested is set. At all other times, the SKP/INT line carries interrupt requests as modified by the HD-6102 interrupt inhibit logic. The flags must always be explicitly cleared by the interrupt service routine.

The DMA transfer rate depends on the program. The minimum rate would be obtained if the processor was executing an auto-indexed DCA or an indirect JMS (even if non-autoindexed, DMA is suppressed during indirect phase of JMS). Continuously executing these instructions would cause DMA transfers to occur only every third memory cycle (IFETCH). The maximum rate could be obtained by executing a “JMP.” loop (JMP to itself); data would be transferred on every cycle and the interrupt routine entered when word count overflows could bump the return address out of the loop.

In dynamic memory systems it should be noted that the MEMSEL* signal narrows when the mode changes from write to refresh (burst mode). RESET signals may need to be limited in duration to prevent loss of memory data in dynamic memory systems.

The accuracy of the clock counter in the programmable real time clock section of the HD-6102 is as follows:

<table>
<thead>
<tr>
<th>CASE</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Counter running; CC loaded from AC via CB using instruction CLAB (IOT 6133) accuracy is 0 to +11 count.</td>
</tr>
<tr>
<td>2</td>
<td>CC loaded from CB automatically on overflow; the accuracy of counting is then only dependent on accuracy of oscillator.</td>
</tr>
</tbody>
</table>

HD-6102 users who do not need all the capabilities of the device may improve systems performance by not using some of the features. To do this properly, certain pins on the device will become unused. The following table summarizes what may be done with certain pins when using only part of the HD-6102 functions. All unlisted pins must be used when implementing any of the three basic features.
## Summary of HD-6102 Instructions

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>I/O CONTROL LINES</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>GTF</td>
<td>6004</td>
<td>SKP 0 0 1</td>
<td>(1) Get Flags</td>
</tr>
<tr>
<td>IOF</td>
<td>6002</td>
<td>C0 0 0</td>
<td>(2) Interrupt Off</td>
</tr>
<tr>
<td>RTF</td>
<td>6005</td>
<td>C1 1 1 1</td>
<td>(3) Restore Flags</td>
</tr>
<tr>
<td>CAF</td>
<td>6007</td>
<td>C2 1</td>
<td>(4) Clear All Flags</td>
</tr>
<tr>
<td>CDF</td>
<td>62N1</td>
<td>Change Data Field</td>
<td></td>
</tr>
<tr>
<td>CIF</td>
<td>62N2</td>
<td>Change Instruction Field</td>
<td></td>
</tr>
<tr>
<td>CDF CIF</td>
<td>62N3</td>
<td>Combination of CDF &amp; CIF</td>
<td></td>
</tr>
<tr>
<td>RDF</td>
<td>6214</td>
<td>Read Data Field</td>
<td></td>
</tr>
<tr>
<td>RIF</td>
<td>6224</td>
<td>Read Instruction Field</td>
<td></td>
</tr>
<tr>
<td>RIB</td>
<td>6234</td>
<td>Read Interrupt Buffer</td>
<td></td>
</tr>
<tr>
<td>RMF</td>
<td>6244</td>
<td>Restore Memory Field</td>
<td></td>
</tr>
<tr>
<td>LIF</td>
<td>6254</td>
<td>Load Instruction Field</td>
<td></td>
</tr>
<tr>
<td>CLZE</td>
<td>6130</td>
<td>Clear Clock Enable Register per AC</td>
<td></td>
</tr>
<tr>
<td>CLSK</td>
<td>6131</td>
<td>Skip on Clock Overflow Interrupt</td>
<td></td>
</tr>
<tr>
<td>CLOE</td>
<td>6132</td>
<td>Set Clock Enable Register per AC</td>
<td></td>
</tr>
<tr>
<td>CLAB</td>
<td>6133</td>
<td>AC to Clock Buffer</td>
<td></td>
</tr>
<tr>
<td>CLEN</td>
<td>6134</td>
<td>Load Clock Enable Register into AC</td>
<td></td>
</tr>
<tr>
<td>CLSA</td>
<td>6135</td>
<td>Clock Status to AC</td>
<td></td>
</tr>
<tr>
<td>CLBA</td>
<td>6136</td>
<td>Clock Buffer to AC</td>
<td></td>
</tr>
<tr>
<td>CLCA</td>
<td>6137</td>
<td>Clock Counter to AC</td>
<td></td>
</tr>
<tr>
<td>LCAR</td>
<td>6205</td>
<td>Load Current Address Register</td>
<td></td>
</tr>
<tr>
<td>RCAR</td>
<td>6215</td>
<td>Read Current Address Register</td>
<td></td>
</tr>
<tr>
<td>LWCR</td>
<td>6225</td>
<td>Load Word Count Register</td>
<td></td>
</tr>
<tr>
<td>LEAR</td>
<td>62N6</td>
<td>Load Extended Current Address Register</td>
<td></td>
</tr>
<tr>
<td>REAR</td>
<td>6235</td>
<td>Read Extended Current Address Register</td>
<td></td>
</tr>
<tr>
<td>LFSR</td>
<td>6245</td>
<td>Load DMA Flags and Status Register</td>
<td></td>
</tr>
<tr>
<td>RSFR</td>
<td>6255</td>
<td>Read DMA Flags and Status Register</td>
<td></td>
</tr>
<tr>
<td>SKOF</td>
<td>6265</td>
<td>Skip on Word Count Overflow</td>
<td></td>
</tr>
<tr>
<td>WRVR</td>
<td>6275</td>
<td>Write Vector Register</td>
<td></td>
</tr>
</tbody>
</table>

### NOTES:
1. The internal flags of the HM-6100 are defined as follows: LINK→AC(0); INTREQ→AC(2); and INTERRUPT ENABLE FF→AC(4).
2. The IOF instruction is used in conjunction with the vector interrupt operation. (See System Considerations.)
3. When RTF is executed, the LINK is restored from AC(0) and the Interrupt System is enabled after the next sequential instruction is executed. The Interrupt Inhibit FF is set preventing interrupts until the next JMP, JMS, or LIF instruction is executed.
4. A hardware RESET clears F7E, WOF, IFF, and COF. The IF and DF are cleared to 0g. The DMA status register, the Clock Enable register, and the Counter/Buffer are cleared.
Summary of HD-6102 Bit Assignments

<table>
<thead>
<tr>
<th>Current Address</th>
<th>DX0</th>
<th>DX1</th>
<th>DX2</th>
<th>DX3</th>
<th>DX4</th>
<th>DX5</th>
<th>DX6</th>
<th>DX7</th>
<th>DX8</th>
<th>DX9</th>
<th>DX10</th>
<th>DX11</th>
</tr>
</thead>
<tbody>
<tr>
<td>CA0</td>
<td>CA1</td>
<td>CA2</td>
<td>CA3</td>
<td>CA4</td>
<td>CA5</td>
<td>CA6</td>
<td>CA7</td>
<td>CA8</td>
<td>CA9</td>
<td>CA10</td>
<td>CA11</td>
<td></td>
</tr>
<tr>
<td>Extended Address</td>
<td>ECA0</td>
<td>ECA1</td>
<td>ECA2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Word Count</td>
<td>WC0</td>
<td>WC1</td>
<td>WC2</td>
<td>WC3</td>
<td>WC4</td>
<td>WC5</td>
<td>WC6</td>
<td>WC7</td>
<td>WC8</td>
<td>WC9</td>
<td>WC10</td>
<td>WC11</td>
</tr>
<tr>
<td>DMA Status (1)</td>
<td></td>
<td>SR5</td>
<td>SR6</td>
<td>SR7</td>
<td>SR8</td>
<td>SR9</td>
<td>SR10</td>
<td>SR11</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interrupt Vector (2)</td>
<td>VR0</td>
<td>VR1</td>
<td>VR2</td>
<td>VR3</td>
<td>VR4</td>
<td>VR5</td>
<td>VR6</td>
<td>VR7</td>
<td>VR8</td>
<td>VR9</td>
<td>VR10</td>
<td>VR11</td>
</tr>
<tr>
<td>RIF Instruction (3)</td>
<td>IF0</td>
<td>IF1</td>
<td>IF2</td>
<td></td>
<td></td>
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<tr>
<td>GTF, RIB Instruction</td>
<td></td>
<td>IB0</td>
<td>IB1</td>
<td>IB2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CDF, RDF Instruction</td>
<td></td>
<td>DF0</td>
<td>DF1</td>
<td>DF2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>RTF Instruction</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock Enable (5)</td>
<td>EN0</td>
<td>EN2</td>
<td>EN3</td>
<td>EN4</td>
<td>EN5</td>
<td>EN7</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>Clock Buffer</td>
<td>CB0</td>
<td>CB1</td>
<td>CB2</td>
<td>CB3</td>
<td>CB4</td>
<td>CB5</td>
<td>CB6</td>
<td>CB7</td>
<td>CB8</td>
<td>CB9</td>
<td>CB10</td>
<td>CB11</td>
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<tr>
<td>Clock Overflow (6)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td></td>
<td>COF</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) DMA STATUS
SR5  Set if Field 7 wraparound carry error — F7E; cleared by CAF, RF5R (at IOTA/AXT time), RESET.
SR6  Set if DMA Word Counter Overflow — WOF; Cleared by CAF, LWCR, RESET.
SR7  Mode Bit 7 
     Cleared by RESET (REFRESH MODE).
SR8  Mode Bit 8 
     See below.
SR9  Carry enable from CA0-11 to ECA2 if set — CE.
SR10 DMA Write if set.
SR11 Enable F7E or WOF interrupt if set — IE.

(2) VR0-10 Loaded from AC. VR11 is equivalent to COF.

(3) IF  Instruction Field; cleared to 0b by RESET and INTGNT.

(4) IIFF Interrupt Inhibit Flip Flop; set whenever IB ≠ IF; (CIF, CDF/CIF, RMF, RTF) cleared by RESET and IB —→ IF transfer.

(5) EN0 Enable Clock Overflow (COF) interrupt; cleared (interrupt disable) by RESET, CAF.

EN2 When set causes clock buffer to be transferred to clock counter on COF. Counter runs at selected rate; COF remains set until cleared with CLSA. When cleared to 0, counter runs at selected rate, overflow occurs every 2^12 counts and COF remains set. EN2 is cleared by RESET, CAF.

EN3,4,5 Select interval between pulses. Cleared to 000 by RESET (counter disabled), CAF see below.

EN7 Inhibits clock prescaler when set. Cleared by RESET, CAF.

(6) COF Clock Overflow status bit; cleared by CAF, RESET and CLSA; complement provides LSB of interrupt vector.

SR7,8 00 Refresh mode; WC is frozen, no UP, DMAEN don’t care.
01 Normal mode; DMAEN (H) freezes WC, CA and no UP if WC has not overflowed; stop if WC overflows.
10 Burst mode; DMAEN (H) freezes WC, CA and no UP if WC has not overflowed; reverts to refresh mode if WC overflows.
11 Stops SDMA

EN3,4,5 with 2MHz clock
000 STOP
001 STOP
010 20ms interval
011 2ms interval
100 200μs interval
101 20μs interval
110 2μs interval
111 STOP

NOTES:
1. Bits SR7 and 8 do not change when the DMA controller stops or reverts to refresh mode as a result of WC overflow.
2. The “overflow” status is defined as set when the most significant bit of a counter makes a “1” to “0” transition.
### HD-6102 Functional Pin Description

<table>
<thead>
<tr>
<th>PIN</th>
<th>SYMBOL</th>
<th>INPUT/OUTPUT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>I</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>2</td>
<td>DMAEN</td>
<td>I</td>
<td>Enable the HM-6102 DMA channel to transfer data</td>
</tr>
<tr>
<td>3</td>
<td>DMAGNT</td>
<td>I</td>
<td>Direct memory access grant from CPU</td>
</tr>
<tr>
<td>4</td>
<td>MEMSEL</td>
<td>I</td>
<td>Memory select for read or write from CPU</td>
</tr>
<tr>
<td>5</td>
<td>IFETCH</td>
<td>I</td>
<td>CPU flag indicating instruction fetch cycle</td>
</tr>
<tr>
<td>6</td>
<td>MEMSEL*</td>
<td>O</td>
<td>Memory select generated by the HM-6102</td>
</tr>
<tr>
<td>7</td>
<td>RESET</td>
<td>I</td>
<td>Asynchronous reset will clear Instruction Field to 0, disable all interrupts, initialize DMA port to READ/REFRESH, initialize timer to &quot;stop&quot;, &quot;divide by 212 mode&quot; and &quot;enable divide counters&quot;</td>
</tr>
<tr>
<td>8</td>
<td>UP</td>
<td>O</td>
<td>User pulse (read or write)</td>
</tr>
<tr>
<td>9</td>
<td>XTA</td>
<td>I</td>
<td>CPU external minor cycle timing signal</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PIN</th>
<th>SYMBOL</th>
<th>INPUT/OUTPUT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>LXMAR</td>
<td>I</td>
<td>A falling edge of LXMAR pulse from CPU will load external memory address register</td>
</tr>
<tr>
<td>11</td>
<td>LXMAR*</td>
<td>O</td>
<td>LXMAR generated by the HM-6102</td>
</tr>
<tr>
<td>12</td>
<td>XTC*</td>
<td>O</td>
<td>XTC generated by the HM-6102</td>
</tr>
<tr>
<td>13</td>
<td>XTC</td>
<td>I</td>
<td>CPU external minor cycle timing signal</td>
</tr>
<tr>
<td>14</td>
<td>CLOCK</td>
<td>I</td>
<td>Oscillator OUT pulses from CPU for timing the HM-6102 DMA transfers</td>
</tr>
<tr>
<td>15</td>
<td>SKP/INTX</td>
<td>I</td>
<td>Multiplexed SKP/INT line from lower priority devices</td>
</tr>
<tr>
<td>16</td>
<td>DX0</td>
<td>I/O</td>
<td>Most significant bit of the 12-bit multiplexed address and data I/O bus</td>
</tr>
<tr>
<td>17</td>
<td>DX1</td>
<td>I/O</td>
<td>See pin 16-DX0</td>
</tr>
<tr>
<td>18</td>
<td>DX2</td>
<td>I/O</td>
<td>See pin 16-DX0</td>
</tr>
<tr>
<td>19</td>
<td>DX3</td>
<td>I/O</td>
<td>See pin 16-DX0</td>
</tr>
<tr>
<td>20</td>
<td>DX4</td>
<td>I/O</td>
<td>See pin 16-DX0</td>
</tr>
</tbody>
</table>

**NOTE:** All DX lines are bi-directional with three-state outputs: Pins 4, 8, 11, 12, 35, 40 have active pullups; pins 32, 33, 34 have open drain outputs; pin 15 has a resistive input pullup; all inputs and outputs protected with resistors and clamp diodes.
HD-6103
CMOS PARALLEL
INPUT/OUTPUT PORT (PIO)

Features

- HM-6100 COMPATIBLE
- LOW POWER - TYP. < 5.0µW STANDBY
- SINGLE SUPPLY 4-11 VOLT
- FULL TEMPERATURE RANGE -55°C TO +125°C
- STATIC OPERATION
- IDEAL FOR MINIMUM SYSTEMS
- 20 PROGRAMMABLE BI-DIRECTIONAL I/O PINS
- THREE MODES OF OPERATION
- SOFTWARE POLLED INTERRUPTS
- UP TO 4 PIO'S PER SYSTEM
- 16 INSTRUCTIONS FOR PIO CONTROL

Description

The HD-6103 Parallel Input/Output Port (PIO) is a high speed, low power, silicon gate CMOS general purpose device which provides parallel data transfers and interrupt control for a variety of peripheral functions, such as displays, keyboards, A/D converters, etc. Data transfers between the HD-6103 are via Input/Output Transfer (IOT) instructions, control lines and DX bus. The PIO is ideal for minimum system configurations.

The HD-6103 has 20 I/O pins that are programmable in groups of 4, 8, or 12 bits via three modes of operation. In one mode, 4 of the pins are utilized as handshake control lines.

Functional Diagram

Pinout

- VCC
- PA7/PC11
- PA6/PC10
- PA5/PC9
- PA4/PC8
- SKP/INT
- PA8/IRS
- PA9/IRE
- CT
- LXMAR
- PA10/ORS
- DEVSEL
- PA11/0RF
- SEL6
- SEL7
- DX0
- DX2
- DX4
- DX1
- DX3
- DX5
- DX6
- DX7
- DX8
- DX10
- PB0
- PB1
- PB2
- PB3
- PB4
- PB5
- PB6
- PB7
- PB8
- PB9
- PB10
- PB11
- PB12
- PB13
- PB14
- PB15
- PB16
- PB17
- PB18
- PB19
- PB20
- PB21
- PB22
- PB23
- PB24
- PB25
- PB26
- PB27
- PB28
- PB29
- PB30
- PB31
- PB32
- PB33
- PB34
- PB35
- PB36
- PB37
- PB38
- PB39
- PB40

2-51
### Specifications HD-6103A

#### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+12.0V</td>
<td>Gnd.</td>
<td>-0.3V</td>
<td>V</td>
<td>0V ≤ VIN ≤ VCC</td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>-0.3V</td>
<td>VCC+0.3V</td>
<td></td>
<td>V</td>
<td>IOH = -0.2mA</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C</td>
<td>150°C</td>
<td></td>
<td>V</td>
<td>0V ≤ VO ≤ VCC</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C</td>
<td>+85°C</td>
<td></td>
<td>V</td>
<td>VIN = VCC, Freq. = 0</td>
</tr>
<tr>
<td>Industrial HD-6103A-9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Military HD-6103A-2</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

#### ELECTRICAL CHARACTERISTICS

VCC = 10.0 ± 0.5% Volts, TA = Industrial or Military

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td></td>
<td>V</td>
<td>V</td>
<td>0V ≤ VIN ≤ VCC</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>20% VCC</td>
<td></td>
<td>V</td>
<td>V</td>
<td>IOH = -0.2mA</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>1.0</td>
<td>1.0</td>
<td>µA</td>
<td>µA</td>
<td>0V ≤ VO ≤ VCC</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Volt.(1)</td>
<td>VCC-2.0</td>
<td></td>
<td>V</td>
<td>V</td>
<td>VIN = VCC, Freq. = 0</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>0.45</td>
<td></td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>µA</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current (static)</td>
<td>1.0</td>
<td>800</td>
<td>µA</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance (2)</td>
<td>5</td>
<td>7</td>
<td>pF</td>
<td>pF</td>
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<tr>
<td>CO</td>
<td>Output Capacitance (2)</td>
<td>8</td>
<td>10</td>
<td>pF</td>
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</tr>
<tr>
<td>CIO</td>
<td>Input/Output Capacitance (2)</td>
<td>8</td>
<td>10</td>
<td>pF</td>
<td>pF</td>
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</tr>
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</table>

Notes:  
(1) Except pins 6, 9  
(2) Guaranteed and sampled, but not 100% tested.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
<th>TEST CONDITIONS</th>
</tr>
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<tbody>
<tr>
<td>tLX</td>
<td>LXMAR Pulse Width</td>
<td>100</td>
<td>ns</td>
<td></td>
<td>CL = 50pF</td>
</tr>
<tr>
<td>tAS</td>
<td>Address Set-Up Time</td>
<td>20</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tAH</td>
<td>Address Hold Time</td>
<td>40</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDC</td>
<td>Delay: DEVSEL to CI</td>
<td>80</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDI</td>
<td>Delay: DEVSEL to SKP/INT</td>
<td>90</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDA</td>
<td>Delay: DEVSEL to DX</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDS</td>
<td>Data Setup Time</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>tDPO</td>
<td>Delay: DEVSEL to Port Data</td>
<td>10</td>
<td>ns</td>
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</tr>
<tr>
<td>tPSLX</td>
<td>Port Data Setup LXMAR</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPHLX</td>
<td>Port Data Hold LXMAR</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPSIR</td>
<td>Port Data Setup IRS</td>
<td>5</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPHIR</td>
<td>Port Data Hold IRS</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPEN</td>
<td>Port B Enable Time</td>
<td>75</td>
<td>ns</td>
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</tr>
<tr>
<td>tPDIS</td>
<td>Port B Disable Time</td>
<td>75</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDR</td>
<td>Delay: IRS to IRE</td>
<td>150</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

A.C.

TA = 26°C  
VCC = 10V
Specifications HD-6103

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+8.0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>Gnd.</td>
<td>-0.3V</td>
<td>+0.3V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6103-9</td>
<td>-65°C</td>
<td></td>
<td>150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military HD-6103-2</td>
<td>-40°C</td>
<td></td>
<td>+85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-55°C</td>
<td></td>
<td>+125°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

VCC = 5.0 ± 10% Volts, TA = Industrial or Military

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical “1” Input Voltage</td>
<td>70%</td>
<td>VCC</td>
<td>V</td>
<td>V</td>
<td>0V ≤ VIN ≤ VCC</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical “0” Input Voltage</td>
<td>20%</td>
<td>VCC</td>
<td>V</td>
<td>V</td>
<td>IOH = -0.2mA</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>µA</td>
<td>VCC</td>
<td>VIN = VCC, Freq. = 0</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical “1” Output Voltage</td>
<td>2.4</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>0V ≤ VO ≤ VCC</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical “0” Output Voltage</td>
<td>0.45</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>IOL = 2.0mA</td>
</tr>
<tr>
<td>IOH</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>µA</td>
<td>VCC</td>
<td>VIN = VCC, Freq. = 0</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current (static)</td>
<td>1.0</td>
<td>100</td>
<td>µA</td>
<td></td>
<td>VIN = VCC, Freq. = 0</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance (2)</td>
<td>5</td>
<td>7</td>
<td>pF</td>
<td></td>
<td>VIN = VCC, Freq. = 0</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance (2)</td>
<td>8</td>
<td>10</td>
<td>pF</td>
<td></td>
<td>VIN = VCC, Freq. = 0</td>
</tr>
<tr>
<td>CIO</td>
<td>Input/Output Capacitance (2)</td>
<td>8</td>
<td>10</td>
<td>pF</td>
<td></td>
<td>VIN = VCC, Freq. = 0</td>
</tr>
</tbody>
</table>

Notes:
1. Except pins 6, 9
2. Guaranteed and sampled, but not 100% tested.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>tLX</td>
<td>LXMAR Pulse Width</td>
<td>200</td>
<td>ns</td>
<td>CL</td>
<td>CL = 50pF</td>
</tr>
<tr>
<td>tAS</td>
<td>Address Setup Time</td>
<td>40</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tAH</td>
<td>Address Hold Time</td>
<td>80</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tDC</td>
<td>Delay: DEVSEL to CI</td>
<td>160</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tDI</td>
<td>Delay: DEVSEL to SKIP/INT</td>
<td>180</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tDA</td>
<td>Delay: DEVSEL to DX</td>
<td>200</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tDS</td>
<td>Data Setup Time</td>
<td>20</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>100</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tDPO</td>
<td>Delay: DEVSEL to Port Data</td>
<td>20</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tPSLX</td>
<td>Port Data Setup LXMAR</td>
<td>20</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tPHLX</td>
<td>Port Data Hold LXMAR</td>
<td>100</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tPSIR</td>
<td>Port Data Setup IRS</td>
<td>10</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tPHIR</td>
<td>Port Data Hold IRS</td>
<td>100</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tPEN</td>
<td>Port B Enable Time</td>
<td>150</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tPDIS</td>
<td>Port B Disable Time</td>
<td>150</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
<tr>
<td>tDR</td>
<td>Delay: IRS to IRE</td>
<td>300</td>
<td>ns</td>
<td></td>
<td>See Timing Diagram</td>
</tr>
</tbody>
</table>

TA = 25°C
VCC = 5.0V

2-53
Specifications HD-6103C-9

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>VCC</td>
<td>5.0±5%</td>
<td>Volts</td>
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<td></td>
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<tr>
<td>Storage Temperature Range</td>
<td>TA</td>
<td>-40°C to +85°C</td>
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<td></td>
<td></td>
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<tr>
<td>Operating Temperature Range</td>
<td>Industrial HD-6103C-9</td>
<td>-65°C to 150°C</td>
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<td></td>
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</table>

ELECTRICAL CHARACTERISTICS

VCC = 5.0±5% Volts, TA = Industrial

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td>.8 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>-10 μA</td>
<td>+10 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIH</td>
<td>Input Leakage</td>
<td>2.4 V</td>
<td>0.45 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>-10 μA</td>
<td>+10 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>-10 μA</td>
<td>+10 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current (static)</td>
<td>1.0 μA</td>
<td>7 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance (2)</td>
<td>5 pF</td>
<td>7 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance (2)</td>
<td>8 pF</td>
<td>10 pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CIO</td>
<td>Input/Output Capacitance (2)</td>
<td>8 pF</td>
<td>10 pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
(1) Except pins 6, 9
(2) Guaranteed and sampled, but not 100% tested.

A.C.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
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<tbody>
<tr>
<td>tLX</td>
<td>LXMAR Pulse Width</td>
<td>230 ns</td>
<td>ns</td>
<td>CL = 50pF</td>
<td></td>
</tr>
<tr>
<td>tAS</td>
<td>Address Setup Time</td>
<td>80 ns</td>
<td>ns</td>
<td>See Timing Diagram</td>
<td></td>
</tr>
<tr>
<td>tAH</td>
<td>Address Hold Time</td>
<td>120 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDC</td>
<td>Delay: DEVSEL to C1 C2</td>
<td>190 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDI</td>
<td>Delay: DEVSEL to SKP/INT</td>
<td>210 ns</td>
<td>ns</td>
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<tr>
<td>tDA</td>
<td>Delay: DEVSEL to DX</td>
<td>250 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDS</td>
<td>Data Setup Time</td>
<td>30 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>120 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDO</td>
<td>Delay: DEVSEL to Port Data</td>
<td>40 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPSLX</td>
<td>Port Data Setup LXMAR</td>
<td>30 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPHLX</td>
<td>Port Data Hold LXMAR</td>
<td>120 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPSIR</td>
<td>Port Data Setup IRS</td>
<td>20 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPHIR</td>
<td>Port Data Hold IRS</td>
<td>120 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPEN</td>
<td>Port B Enable Time</td>
<td>175 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPDIS</td>
<td>Port B Disable Time</td>
<td>175 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDR</td>
<td>Delay: IRS to IRE ORS to ORF</td>
<td>340 ns</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

D.C.
The three-state bi-directional 12-bit DX bus is used to transfer data and control information (Fig. 3) between the HD-6103 and the HM-6100 microprocessor. The HM-6100 transmits the device address and control information on the DX bus during the ‘execute’ phase of an Input-Output Transfer (IOT) instruction. The HD-6103 accepts this information on the falling edge of the LXMAR (AddressLatch Enable) Signal.

The address bits (6-7) are compared with the chip select inputs (SEL6 and SEL7) to address 1 of 4 PIO’s. The IOT address bits (3-5) are programmed internally to respond to the bit pattern 011. The SEL6 and SEL7 inputs should be externally hard-wired to match the DX6 and DX7 chip select bits. As shown in Fig. 3, DEVSEL goes low, during the first half of an IOT execute machine cycle for a read operation and it goes low again in the second half for a write operation. The HD-6103 responds to a ‘read’ instruction by putting data on the DX bus and C1 output (of HM-6100) low when DEVSEL (from HM-6100) input is low. C1 line goes low to indicate an input transfer cycle to the HM-6100. All PIO data transfers to the HM-6100 Accumulator (AC) is an ‘OR’ transfer, (i.e., PIO data is OR’ed into the contents of the AC).
During the write operation into PIO, the PIO accepts data from the HM-6100 Accumulator on the rising edge of the DEVSEL. During and after the PIO write, the contents of the accumulator are not cleared.

SKP/INT line goes low during the 'read' DEVSEL if the HD-6103 is responding to a 'skip' instruction, and the 'skip' condition is met, therefore causing the HM-6100 to skip the next sequential instruction. SKP/INT line reflects the interrupt request status of the HM-6100 at all times except during the 'read' DEVSEL. The SKP/INT line goes low if an active interrupt request is pending. During read DEVSEL mode, the SKP/INT indicates the current skip condition. The bits are interpreted as shown below:

Note: Both CI and SKP/INT are open drain outputs which are wire OR'd with outputs from other HM-6100 peripheral controllers.

The HD-6103 has 20 I/O pins which can be individually programmed in groups of 4, 8 or 12 bits in three different modes of operation.

In mode 11, the 20 I/O lines are divided into three ports:
- Port A with 4 bits (PA8 - PA11)
- Port B with 12 bits (PB0 - PB11)
- Port C with 4 bits (PC8 - PC11)

In mode 10, the 20 I/O lines are grouped into 2 ports:
- Port A with 8 bits (PA4 - PA11)
- Port B with 12 bits (PB0 - PB11)

The four I/O lines associated with Port C in Mode 11 (PC8 - PC11) are allocated to Port A as PA4 - PA7.

In mode 0X, there are two ports - Port B with 12 bits and Port C with 4 bits and four lines for handshake control logic. Four lines of Port A in Mode 11 (PA8 - PA11) are reassigned as handshake control lines. They are:
- Input Register Strobe (IRS)
- Input Register Empty (IRE)
- Output Register Strobe (ORS)
- Output Register Empty (ORE)

The handshake logic controls the data transfer for the Port B. Port C operation remains the same as in Mode 11.

For an 'input' transfer in 0X Mode, the input register empty (IRE) output goes high to indicate to the peripheral device that the input register is empty (as shown in Fig. 4).
The peripheral device may then strobe in the new data into Port B with Input Register Strobe (IRS). At this time, IRE goes low to indicate to the peripheral device that the input buffer is full, and remains low until Port B has been read by the HM-6100 microprocessor. IRE then goes high after the HM-6100 executes a Read Port B (RPB) instruction to initiate another input sequence. The data into Port B should be valid only for a short duration before and after IRS makes the 1 to 0 transition.

![Figure 4: Input Data Transfer (Peripheral device to PIO)](image)

For an ‘output’ transfer in OX mode, the HM-6100 microprocessor writes the data into Port B and its timing is shown in Fig. 5. ORF line from the PIO goes high, signaling the peripheral device that the output register is full. The peripheral device may then strobe in the new data from Port B with ORS. Port B stays in the high impedance mode until ORS is activated by the peripheral device. ORF line goes low and remains low until Port B has been written into by the HM-6100 microprocessor. ORF then goes high, initiating another output sequence.

![Figure 5: Output Data Transfer (PIO to peripheral device)](image)

The HM-6100 monitors the status of ORF (Output Register Full). If it is low (i.e., output register is empty), HM-6100 may load data into Port B output buffer with SPB/ CPB/WPB instruction. ORF goes high a delay time after the rising edge of the ‘write’ DEVSEL, signaling the peripheral device that output buffer has new data. During this time, Port B output buffers remain three-stated. The peripheral device may then enable and read out Port B output latches by activating ORS (Output Register Strobe) high. The falling edge of ORS (from high to low) signals the PIO that the peripheral device no longer needs the valid current information. Port B is three-stated and ORF then goes low, thereafter, to indicate another output sequence.

ORF should be set to 0 and IRE to 1 with a ‘write’ command in Mode OX, to initiate the handshaking sequence.

The HM-6100 microprocessor should not write into Port B until ORF is low for an ‘output’ transfer and should not read Port B until IRE is low for an ‘input’ transfer. The peripheral device reads Port B if ORF is high and writes into Port B if IRE is high.

The PIO may be programmed to generate an INTREQ (Interrupt Request) to the microprocessor when ORF or IRE goes low by setting the respective Interrupt enable bits, OREN and IREN.

The HM-6100 may poll the status of ORF or IRE by executing the respective skip instructions SKPOR and SKPIR, by reading the status register or by reading “Port A”.

In Mode 11 and 10, when handshaking control is not in effect, the execution of SKPOR and SKPIR Instructions depend on the state of the Port A lines PA11 and PA9, respectively. The Interrupt feature is available only in Mode OX.

The mode of operation - 11, 10 or 0X, is selected by programming the Status Register (SR).

All ports are bi-directional. The execution of a ‘write’ instruction caused a port to be automatically programmed to be an ‘output’. The output data may be changed by using the ‘set’, ‘clear’ or ‘write’ instructions. The output remains valid until the port bit lines are reset to be inputs.

Execution of a ‘read’ instruction causes a port to be automatically set as an ‘input’ port – i.e., it presents a very high impedance to the I/O lines. Data appearing on the I/O lines will be sampled into the port input latch at every LXMAR pulse and may be read by the HM-6100 microprocessor by the ‘read’ instruction.
In Mode OX, Port B acts as a three-state bi-directional buffer which is controlled by an external peripheral device. ORF and IRE lines are outputs and ORS and IRS lines are inputs.

At power-on, all ports are defined to be input ports and the PIO is initialized to be in Mode 10. With 20 I/O lines partitioned into the 8/12 (i.e., Port A = 8 bits, Port B = 12 bits) format.

### PIO Instructions

<table>
<thead>
<tr>
<th>PIO CONTROL</th>
<th>MNE-MONICS</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>SETPA</td>
<td>Set PA(i) to 1 if AC(i) is 1. AC is not cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 11: PA(i) ← PA(i) + AC(i), 8 ≤ i ≤ 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 10: PA(i) ← PA(i) + AC(i), 4 ≤ i ≤ 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 0X: IREN ← IREN + AC(B)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRE ← IRE + AC(9)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OREN ← OREN + AC(10)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ORF ← ORF + AC(11)</td>
</tr>
<tr>
<td>0001</td>
<td>CLRPA</td>
<td>Clear Port A. Clear PA(i) to 0 if AC(i) is 1. AC is not cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 11: PA(i) ← PA(i) ∨ AC(i), 8 ≤ i ≤ 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 10: PA(i) ← PA(i) ∨ AC(i), 4 ≤ i ≤ 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 0X: IREN ← IREN ∨ AC(B)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRE ← IRE ∨ AC(9)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ORF ← ORF ∨ AC(11)</td>
</tr>
<tr>
<td>0010</td>
<td>WPA</td>
<td>Write Port A. Set PA(i) ← AC(i). AC is not cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 11: PA(i) ← AC(i), 8 ≤ i ≤ 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 10: PA(i) ← AC(i), 4 ≤ i ≤ 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 0X: IREN ← AC(B)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IRE ← AC(9)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ORF ← AC(10)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ORF ← AC(11)</td>
</tr>
<tr>
<td>0011</td>
<td>RPA</td>
<td>Read Port A. 'OR' transfer PA to AC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 11: AC(i) ← AC(i) + PA(i), 8 ≤ i ≤ 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(i) ← AC(i), 0 ≤ i ≤ 7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 10: AC(i) ← AC(i) + PA(i), 4 ≤ i ≤ 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 0X: AC(i) ← AC(i) + IRS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(9) ← AC(9) + IRE</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(10) ← AC(10) + ORS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(11) ← AC(11) + ORF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(i) ← AC(i), 0 ≤ i ≤ 11</td>
</tr>
<tr>
<td>0100</td>
<td>SETPB</td>
<td>Set Port B. Set PB(i) to 1 if AC(i) is 1. AC is not cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PB(i) ← PB(i) + AC(i), 0 ≤ i ≤ 11</td>
</tr>
<tr>
<td>0101</td>
<td>CLRPB</td>
<td>Clear Port B. Clear PB(i) to 0 if AC(i) is 1. AC is not cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PB(i) ← PB(i) ∨ AC(i), 0 ≤ i ≤ 11</td>
</tr>
<tr>
<td>0110</td>
<td>WPB</td>
<td>Write Port B. Set PB(i) ← AC(i). AC is not cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>PB(i) ← AC(i), 0 ≤ i ≤ 11</td>
</tr>
<tr>
<td>0111</td>
<td>RPB</td>
<td>Read Port B. 'OR' transfer PB to AC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(i) ← AC(i) + PB(i), 0 ≤ i ≤ 11</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PIO CONTROL</th>
<th>MNE-MONICS</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>SETPC</td>
<td>Set Port C. Set PC(i) to 1 if AC(i) is 1. AC is not cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 11 and OX: PC(i) ← PC(i) + AC(i)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 10: No operation</td>
</tr>
<tr>
<td>1001</td>
<td>CLRPC</td>
<td>Clear Port C. Clear PC(i) to 0 if AC(i) is 1. AC is cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 11 and OX: PC(i) ← PC(i) ∨ AC(i)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 10: No operation</td>
</tr>
<tr>
<td>1010</td>
<td>WPC</td>
<td>Write Port C. Set PC(i) = AC(i). AC is not cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 11 and OX: AC(i) ← AC(i)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 10: No operation.</td>
</tr>
<tr>
<td>1111</td>
<td>RSR</td>
<td>Read Status Register. 'OR' transfer Status Register to AC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(i) ← AC(i), 0 ≤ i ≤ 11</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(8) ← AC(8) + M(8)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(9) ← AC(9) + M(9)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 11 and 10: AC(10) ← AC(10) + PA(11)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(11) ← AC(11) + PA(9)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Mode 0X: AC(10) ← AC(10) + ORINT</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AC(11) ← AC(11) + IRINT</td>
</tr>
</tbody>
</table>

Symbol definition: ∧ “and” + “or” → “is replaced by”
FIGURE 6 – HD-6103 PIO Register Bit Assignments

| Pins | 2 | 3 | 4 | 5 | 7 | 8 | 11 | 13 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 |
|------|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Mode 10 | PA7 | PA6 | PA5 | PA4 | PA8 | PA9 | PA10 | PA11 | PB0 | PB1 | PB2 | PB3 | PB4 | PB5 | PB6 | PB7 | PB8 | PB9 | PB10 | PB11 |
| Mode 11 | PC11 | PC10 | PC9 | PC8 | PA8 | PA9 | PA10 | PA11 | PB0 | PB1 | PB2 | PB3 | PB4 | PB5 | PB6 | PB7 | PB8 | PB9 | PB10 | PB11 |
| Mode OX | PC11 | PC10 | PC9 | PC8 | IRS | IRE | ORS | ORF | PB0 | PB1 | PB2 | PB3 | PB4 | PB5 | PB6 | PB7 | PB8 | PB9 | PB10 | PB11 |

FIGURE 7 – HD-6103 PIO Port Pin Assignments
The Status Register (SR) has 2 mode bits, M8 and M9 which can be modified by the WSR (Write Status Register) instruction. These two bits define the mode of operation for the HD-6103 as shown in Figure 8.

<table>
<thead>
<tr>
<th>M8</th>
<th>M9</th>
<th>MODE</th>
<th>PORT OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>*</td>
<td>Mode 0X</td>
<td>PB(0)-(11), PC(8)-(11), IRS, IRE, ORS, ORF</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Mode 10</td>
<td>PB(0)-(11), PA(4)-(11)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Mode 11</td>
<td>PB(0)-(11), PC(8)-(11), PA(8)-(11)</td>
</tr>
</tbody>
</table>

**FIGURE 8 – Mode Bit Assignments**

The Mode and Interrupt status bits, ORINT (Output Register empty Interrupt) and IRINT (Input Register empty Interrupt), may be read with the RSR (Read Status Register) instruction. The interrupt status bits are set to 0 if the corresponding flag is requesting an interrupt.

In Mode 11/10 the current value of PA11 and PA9 can be interrogated. In this mode, Port A can be either an input or an output. M(8) and M(9) are initialized to ‘11’ at power-on.

**FIGURE 9 – Status Register Bit Assignments**

**SKIP OPERATION**

The HM-6100 may poll the status of ORF or IRE in Mode 0X, by executing a skip instruction, SKPOR or SKPIR. The HD-6103 will assert the SKP/INT line low if the corresponding status line (ORF or IRE) is low, causing the next sequential instruction to be skipped. During this cycle, ORF and IRE remain unchanged.

In Mode 11/10, SKPOR and SKPIR instruction executions depend on the state of PA11 and PA9, respectively. Port A may be an input or output port.

If ORF is reset to 0 be executing a CLRPA or WPA instruction to initiate the handshaking sequence, the next SKPOR instruction will cause the next sequential instruction to be skipped.

**INTERRUPT OPERATION**

The HD-6103 may be programmed to generate an interrupt request input (INTREQ) when ORF or IRE goes low, by setting the corresponding interrupt enable bits, OREN or IREN, to 1. If the HM-6100 interrupt system has been previously enabled, the microprocessor will acknowledge the INTREQ input. If the HM-6100 microprocessor does not see the higher priority INTREQ’s, inputs from other peripheral controllers such as HD-6102 Memory Extender/Direct Memory Access/Internal Timer Controller (MEDIC) or HD-6101 Parallel Interface Elements (PIE) in the system, the interrupt service routine should initiate a software poll of the PIO’s in the system to identify the particular PIO that generated the INTREQ. In Mode 0X, the interrupt request status of ORF and IRE may be identified by reading the Status Register. ORINT or IRINT will be set to 0 if ORF (being low) or IRE (being low) is generating an INTREQ. Note that HD-6102 MEDIC and HD-6101 PIE provide an automatic priority vectoring.

The interrupt feature of HD-6103 is available only in Mode 0X. An ORF INTREQ may be removed by one of the following methods:

- Executing an SPB/CPB/WPB Instruction (ORF goes high if Port B is written into), or
- Setting ORF to 1 with SPA/WPA Instruction, or
- By resetting OREN to 0 with a CPA/WPA Instruction, or
- By changing to Mode 11/10.

An IRE INTREQ may be removed by:

- Executing a RPB Instruction (IRE goes higher after Port B is read), or
- Setting IRE to 1 with SPA/WPA Instruction, or
- Resetting IREN to 0 with a CPA/WPA Instruction, or

PIO may be software programmed to generate an INTREQ to the HM-6100 by resetting ORF or IRE to 0 with a CPA/WPA Instruction and by setting the corresponding enable bit, OREN or IREN, with a SPA/WPA Instruction in Mode 0X.
## PIN DEFINITIONS

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>SYMBOL</th>
<th>INPUT/OUTPUT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td></td>
<td>Positive Power Supply</td>
</tr>
<tr>
<td>2</td>
<td>PA7</td>
<td>I/O</td>
<td>Port A I/O Line (7)</td>
</tr>
<tr>
<td>3~5</td>
<td>PA6~PA4</td>
<td>I/O</td>
<td>Port A6~A4 (Mode 10)</td>
</tr>
<tr>
<td>6</td>
<td>SKP/INT</td>
<td>O</td>
<td>Time Multiplexed SKP and INTREQ lines to the HM-6100 Microprocessor — Active Low. This output is open drain.</td>
</tr>
<tr>
<td>7</td>
<td>PA8</td>
<td>I/O</td>
<td>Port A I/O Line in Mode 11/10 — Most Significant Bit of Port A in Mode 11.</td>
</tr>
<tr>
<td>8</td>
<td>PA9</td>
<td>I/O</td>
<td>Port A9 (Mode 11/10).</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>SYMBOL</th>
<th>INPUT/OUTPUT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>CT</td>
<td>O</td>
<td>C1 output goes low upon completion of PIO Port data transfer to the HM-6100 Accumulator (AC). This output is an open-drain output to be wired-OR'd with CT lines from other HM6100 peripheral controllers.</td>
</tr>
<tr>
<td>10</td>
<td>LXMAR</td>
<td>I</td>
<td>Address Latch enable signal from the HM-6100. PIO clocks in address and control information from the HM-6100 on the falling edge of LXMAR. All Port inputs are sampled at LXMAR.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>SYMBOL</th>
<th>INPUT/OUTPUT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>PA10</td>
<td>I/O</td>
<td>Port A10 (Mode 11/10).</td>
</tr>
<tr>
<td></td>
<td>ORS</td>
<td>I</td>
<td>Output Register Strobe input to Enable Port B output buffers in Mode 0X. Port B is three-stated when ORS is low.</td>
</tr>
<tr>
<td>12</td>
<td>DEVSEL</td>
<td>I</td>
<td>Input-Output Device Select control line from the HM-6100. It performs both the read and write function. The first negative transition after LXMAR, enables the DX output buffer of the selected PIO for a read operation. When DEVSEL returns high, the 'read' operation is terminated. The second negative-going pulse on DEVSEL serves as a 'write' pulse to the selected PIO and the HM-6100 AC data is written into the selected PIO register or port on the rising edge.</td>
</tr>
<tr>
<td>13</td>
<td>PA11</td>
<td>I/O</td>
<td>Port A11 (Mode 11/10)—Least Significant bit of Port A.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>SYMBOL</th>
<th>INPUT/OUTPUT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>ORF</td>
<td>O</td>
<td>Output Register Full output goes high when the HM-6100 writes into Port B in a handshake mode. It goes low when the peripheral device reads Port B by enabling ORS high. The PIO may be programmed to generate an INTREQ on ORF (Mode 0X).</td>
</tr>
<tr>
<td>14</td>
<td>SEL6</td>
<td>I</td>
<td>A Chip Select Input. PIO has 2 chip selects, SEL6 and SEL7, thereby enabling up to 4 PIO chips in a system.</td>
</tr>
<tr>
<td>15</td>
<td>SEL7</td>
<td>I</td>
<td>A Chip Select Input.</td>
</tr>
<tr>
<td>16~25</td>
<td>DX0~DX9</td>
<td>I/O</td>
<td>The HM-6100 System bus (Data and Address).</td>
</tr>
<tr>
<td>26</td>
<td>GND</td>
<td></td>
<td>Ground</td>
</tr>
<tr>
<td>27~28</td>
<td>DX10~DX11</td>
<td>I/O</td>
<td>HM-6100 System bus (Data and Address).</td>
</tr>
<tr>
<td>29~40</td>
<td>PB0~PB11</td>
<td>I/O</td>
<td>I/O Port Pin. PB0 is the most Significant bit, and PB11 is the Least Significant bit.</td>
</tr>
</tbody>
</table>
# IOT Considerations

The HM-6100 communicates with peripherals via input/output transfers (IOT) instructions. The first three bits, 0-2 are always set to 68 (110) to specify an IOT instruction. The next 9 bits, 3-11, are user definable and can provide a minimal implementation when each bit controls one operation. When following PDP-8/E format, the next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permits interfaces with up to 63 I/O devices. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The HD-6102 MEDIC utilizes the PDP-8/E format. When using the HD-6101 PIE and the HD-6103 PIO, bits 3-7 perform the device selection function and bits 8-11 provide the operation specification code.

## IOT Instruction Format

### IOT Instruction Format

<p>| | | | | | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
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</tr>
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<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
<td>11</td>
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</table>

**USER DEFINABLE BITS**

**Basic IOT Instruction:** 6XXXg

<p>| | | | | | | | | | | | |</p>
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<tr>
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<td>3</td>
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<td>7</td>
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</table>

**DEVICE SELECTION**

**CONTROL**

**PDP-8/E Format:** 6NNXg

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</tbody>
</table>

**DEVICE SELECTION**

**CONTROL**

**PIE and PIO Format**

Care must be taken when building a system which uses all three peripheral interface devices from Harris to avoid conflicts with the device selection codes. Care also must be used when utilizing DEC compatible teletype and high speed reader interfaces in a system which includes PIE’s and PIO’s. The following table will assist in the assignment of device selection codes.
<table>
<thead>
<tr>
<th>PDP-8/E ①</th>
<th>PIE &amp; PIO ②</th>
<th>DEVICE TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>000 00</td>
<td>Internal IOT's</td>
</tr>
<tr>
<td>01</td>
<td>000 00</td>
<td>DEC High Speed Reader</td>
</tr>
<tr>
<td>02</td>
<td>000 01</td>
<td>DEC High Speed Punch</td>
</tr>
<tr>
<td>03</td>
<td>000 01</td>
<td>DEC Teletype Keyboard/Reader</td>
</tr>
<tr>
<td>04</td>
<td>000 10</td>
<td>DEC Teletype Printer/Punch</td>
</tr>
<tr>
<td>05</td>
<td>000 10</td>
<td>User Definable (DEC PDP-8/E Format Only)</td>
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<tr>
<td>06, 07</td>
<td>000 11</td>
<td>User Definable</td>
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<td>10, 11</td>
<td>001 00</td>
<td>User Definable</td>
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<td>12</td>
<td>001 01</td>
<td>User Definable (DEC PDP-8/E Format Only)</td>
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<tr>
<td>13</td>
<td>001 01</td>
<td>MEDIC Real Time Clock</td>
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<tr>
<td>14, 15</td>
<td>001 10</td>
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<td>16, 17</td>
<td>001 11</td>
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<td>010 00</td>
<td>MEDIC Extended Memory Control and DMA</td>
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<td>010 01</td>
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<td>010 10</td>
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<td>26, 27</td>
<td>010 11</td>
<td>MEDIC Extended Memory Control and DMA</td>
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<tr>
<td>30, 31</td>
<td>011 00</td>
<td>HD-6103 PIO No. One</td>
</tr>
<tr>
<td>32, 33</td>
<td>011 01</td>
<td>HD-6103 PIO No. Two</td>
</tr>
<tr>
<td>34, 35</td>
<td>011 10</td>
<td>HD-6103 PIO No. Three</td>
</tr>
<tr>
<td>36, 37</td>
<td>011 11</td>
<td>HD-6103 PIO No. Four</td>
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<td>40, 41</td>
<td>100 00</td>
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<td>60, 61</td>
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<td>72, 73</td>
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<td>111 10</td>
<td></td>
</tr>
<tr>
<td>76, 77</td>
<td>111 11</td>
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</tbody>
</table>

**NOTES:**

① PDP-8/E device selection in octal.
② PIE & PIO device selection in binary.
## CMOS Memory Family

<table>
<thead>
<tr>
<th>Symbols and Abbreviations</th>
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</tr>
</thead>
<tbody>
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<td>Battery Backup Applications</td>
<td>3–3</td>
</tr>
<tr>
<td><strong>CMOS ROM</strong></td>
<td></td>
</tr>
<tr>
<td>HM-6312 1024 x 12</td>
<td>3–4</td>
</tr>
<tr>
<td><strong>CMOS RAMS</strong></td>
<td></td>
</tr>
<tr>
<td>HM-6512 64 x 12</td>
<td>3–10</td>
</tr>
<tr>
<td>HM-6561 256 x 4</td>
<td>3–15</td>
</tr>
<tr>
<td>HM-6518 1024 x 1</td>
<td>3–20</td>
</tr>
<tr>
<td>HM-6533 1024 x 4</td>
<td>3–25</td>
</tr>
<tr>
<td>HM-6543 4096 x 1</td>
<td>3–31</td>
</tr>
</tbody>
</table>
Symbols and Abbreviations

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe that, once acclimated, you will find this standardized format easy to read and use.

**ELECTRICAL PARAMETER ABBREVIATIONS**

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

- V (Voltage)
- I (Current)
- P (Power)
- C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates the high (H), low (L) or off (Z) state of the pin during measurements. Examples:

- VIL - Input Low Voltage
- IOZ - Output Leakage Current

**TIMING PARAMETER ABBREVIATIONS**

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a “from-to” sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

- T X X X

  Signal name from which interval is defined
  Transition direction for first signal
  Signal name to which interval is defined
  Transition direction for second signal

**Signal Definitions:**

- A = Address
- D = Data In
- Q = Data Out
- W = Write Enable
- E = Chip Enable
- S = Chip Select
- G = Output Enable

**Transition Definitions:**

- H = Transition to High
- L = Transition to Low
- V = Transition to Valid
- X = Transition to Invalid or Don’t Care
- Z = Transition to Off (High Impedance)

**EXAMPLE:**

1. **CHIP ENABLE E**

   ![Diagram of CHIP ENABLE](image)

   - TWLEH - Time from Write enable Low to chip Enable High.

**TIMING LIMITS**

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

**WAVEFORMS**

<table>
<thead>
<tr>
<th>WAVEFORM SYMBOL</th>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Waveform Icon" /></td>
<td>MUST BE VALID</td>
<td>WILL BE VALID</td>
</tr>
<tr>
<td><img src="image" alt="Waveform Icon" /></td>
<td>CHANGE FROM H TO L</td>
<td>WILL CHANGE FROM H TO L</td>
</tr>
<tr>
<td><img src="image" alt="Waveform Icon" /></td>
<td>CHANGE FROM L TO H</td>
<td>WILL CHANGE FROM L TO H</td>
</tr>
<tr>
<td><img src="image" alt="Waveform Icon" /></td>
<td>DON'T CARE: ANY CHANGE PERMITTED</td>
<td>CHANGING: STATE UNKNOWN</td>
</tr>
<tr>
<td><img src="image" alt="Waveform Icon" /></td>
<td></td>
<td>HIGH IMPEDANCE</td>
</tr>
</tbody>
</table>
Battery Backup Applications

The Harris CMOS Memories are especially well suited for use in battery backup systems. Data retention supply voltage and supply current are guaranteed over the full temperature range.

When designing the backup system, the following suggestions should be considered:

1. As RAM VCC drops, the input logical one voltages should follow so as not to exceed VCC +0.3. It is suggested to use CMOS drivers, operating at CMOS VCC, such as the HD-6495, HD-6432, and HD-6433. Another approach is the use of open collector or open drain buffers pulled up to CMOS VCC.

2. E must be held high at CMOS VCC and S, G high or G low. W, G, address, and data inputs should be held at either GND or CMOS VCC.

3. When exiting from the battery backup mode, VCC should ramp without ring or discontinuities.

4. The RAM can begin operation one TEHEL after VCC reaches the minimum operating voltage (4.5 or 4.75V).

A very simple battery backup system is shown in Figure 1. When system power is available, diode D1 is forward biased and supplies current to the CMOS devices. Upon loss of system power, diode D1 is reversed biased and only CMOS devices are consuming battery power. A disadvantage to this method is that CMOS VCC is one diode drop .7V, below TTL VCC. There is a possibility that a TTL output signal could rise higher than CMOS VCC and cause possible latch problems. This possibility can be reduced by incorporating a system similar to that shown in Figure 2. Other alternatives include using a germanium diode yielding a VF ≈ .2V or adding diode D2 in the TTL supply and raising VCC to account for the drop. A PNP transistor is substituted for the diode in Figure 2. The saturation drop of the transistor, 0.2V, is less than the 0.7V drop of the diode giving more margin against latch-up. A power fail output signal is available to disable the E circuitry. Open collector TTL with pullups to CMOS VCC or LS type TTL should be used as memory drivers. This will insure that the CMOS inputs are not floating during the backup period. When system power is restored, operation continues as normal and the NI-CAD battery pack is trickle charged through RC.

**FIGURE 1**

**FIGURE 2**
Features

- HM-6100 COMPATIBLE
- LOW POWER - TYPICAL < 5.0 µW STANDBY
- 4 – 11 VOLT VCC OPERATION
- HIGH SPEED
- STATIC OPERATION

Description

The HM-6312 and HM-6312A are high speed, low power, silicon gate CMOS static ROM's, organized 1024 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. The basic part operates at 4 – 7 volts with a typical 5 volt 25°C access time of 350ns. Higher operating voltages, 4 – 11 volts, are available with the A version. Signal polarities and functions are specified for interfacing with the HM-6100 Microprocessor.

Operation

Addresses and data out are multiplexed on 12 lines, DX0 – DX11. Addresses are loading into an on chip register by falling edge of E. Data out, corresponding to the latched address, is enabled when E, G and G are true. The F output defines an area in the 4096 word addressing space dedicated to RAM. It can be programmed by DX0, DX1, DX2 and DX3. This output eliminates a four bit register and decoder for the high order address bits to select RAM.

Functional Diagram
Specifications HM-6312A-2/HM-6312A-9

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+12.0V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Applied Input or Output Voltage</td>
<td>GND -0.3V to VCC + 0.3V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Industrial-9</td>
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<td></td>
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<tr>
<td>Military-2</td>
<td></td>
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**ELECTRICAL CHARACTERISTICS**  
VCC = 10 ± 5%

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<tr>
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<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td></td>
<td></td>
<td>20% VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IIIL</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td></td>
<td>+1.0</td>
<td>μA</td>
<td>0V ≤ VIN ≤ VCC</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td></td>
<td></td>
<td>VCC -0.1</td>
<td>V</td>
<td>IOUT = 0</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td></td>
<td></td>
<td>GND + 0.1</td>
<td>V</td>
<td>IOUT = 0</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td></td>
<td>1.0</td>
<td>μA</td>
<td>0V ≤ VO ≤ VCC</td>
</tr>
<tr>
<td>ICCSB</td>
<td>Standby Supply Current</td>
<td></td>
<td></td>
<td>800</td>
<td>μA</td>
<td>VIN = 0 or VCC</td>
</tr>
<tr>
<td>ICCOP</td>
<td>Operating Current</td>
<td>7</td>
<td></td>
<td>10</td>
<td>mA</td>
<td>f = 1MHz, IO = 0</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>5.0</td>
<td></td>
<td>7.0</td>
<td>pF</td>
<td>VI = VCC or GND</td>
</tr>
<tr>
<td>CIO</td>
<td>I/O Capacitance</td>
<td>6.0</td>
<td></td>
<td>10.0</td>
<td>pF</td>
<td></td>
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**INDUSTRIAL** | **MILITARY**

<table>
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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>TELQV</td>
<td>Access Time From E</td>
<td>200</td>
<td></td>
<td></td>
<td>220</td>
<td>ns</td>
<td>VCC = 10 ± 5%</td>
</tr>
<tr>
<td>TGHQV</td>
<td>Output Enable Time</td>
<td>160</td>
<td></td>
<td></td>
<td>175</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TGLOZ</td>
<td>Output Disable Time</td>
<td>160</td>
<td></td>
<td></td>
<td>175</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TEHEL</td>
<td>Strobe Pos. Pulse Width</td>
<td>125</td>
<td></td>
<td></td>
<td>140</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TELQ</td>
<td>Cycle Time</td>
<td>325</td>
<td></td>
<td></td>
<td>360</td>
<td>ns</td>
<td></td>
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<tr>
<td>TAVEL</td>
<td>Address Set-Up Time</td>
<td>30</td>
<td></td>
<td></td>
<td>35</td>
<td>ns</td>
<td></td>
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<tr>
<td>TELAX</td>
<td>Address Hold Time</td>
<td>55</td>
<td></td>
<td></td>
<td>60</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TELFV</td>
<td>Propagation to F</td>
<td>100</td>
<td></td>
<td></td>
<td>110</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 7mA/MHz.
2. Capacitance sampled and guaranteed – not 100% tested.
3. A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs - 1TTL Load and 50pF.
Specifications HM-6312-2/HM-6312-9

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+8</td>
<td></td>
<td>0V</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Applied Input or Output Voltage</td>
<td>-0.3V to VCC + 0.3V</td>
<td>GND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td>Industrial-9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
<td>Military-2</td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**ELECTRICAL CHARACTERISTICS**

VCC = 5 ± 10%

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>Typ</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical “1” Input Voltage</td>
<td>70%</td>
<td></td>
<td>VCC</td>
<td>V</td>
<td>0V ≤ VIN ≤ VCC</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical “0” Input Voltage</td>
<td>-1.0</td>
<td></td>
<td>20%</td>
<td>µA</td>
<td>IOUT = 0</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td></td>
<td>+1.0</td>
<td>µA</td>
<td>IOUT = 0</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical “1” Output Voltage</td>
<td>VCC</td>
<td></td>
<td>-0.1</td>
<td>V</td>
<td>0V ≤ VO ≤ VCC</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical “0” Output Voltage</td>
<td>GND</td>
<td></td>
<td>+0.1</td>
<td>µA</td>
<td>VI = 0 or VCC</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td></td>
<td>1.0</td>
<td>µA</td>
<td>VI = VCC or GND</td>
</tr>
<tr>
<td>ICCSB</td>
<td>Standby Supply Current</td>
<td>3</td>
<td>5</td>
<td>100</td>
<td>mA</td>
<td>f = 1MHz, IO = 0</td>
</tr>
<tr>
<td>ICCOP</td>
<td>Operating Current</td>
<td>3</td>
<td>5</td>
<td>100</td>
<td>µA</td>
<td>VI = 0 or VCC</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>5.0</td>
<td>7.0</td>
<td>pF</td>
<td></td>
<td>VI = VCC or GND</td>
</tr>
<tr>
<td>CIO</td>
<td>I/O Capacitance</td>
<td>6.0</td>
<td>10.0</td>
<td>pF</td>
<td></td>
<td>VI = VCC or GND</td>
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</tbody>
</table>

See Switching Waveforms page 3-8

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>ININDUSTRIAL</th>
<th>MILITARY</th>
<th>MIN</th>
<th>MAX</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TELQV</td>
<td>Access Time From E</td>
<td>510</td>
<td>560</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>VCC = 5 ± 10%</td>
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<tr>
<td>TGHOV</td>
<td>Output Enable Time</td>
<td>290</td>
<td>320</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGLOZ</td>
<td>Output Disable Time</td>
<td>290</td>
<td>320</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEHEL</td>
<td>Strobe Pos. Pulse Width</td>
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<td>ns</td>
<td></td>
<td></td>
<td></td>
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<td>TELEL</td>
<td>Cycle Time</td>
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<td>845</td>
<td>ns</td>
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<td>ns</td>
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<td>Address Hold Time</td>
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<td>135</td>
<td>ns</td>
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<td></td>
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</tr>
<tr>
<td>TELFV</td>
<td>Propagation to F</td>
<td>220</td>
<td>240</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
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</table>

NOTES: ① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 3mA/MHz.
② Capacitance sampled and guaranteed - not 100% tested.
③ A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs -1TTL Load and 50pF.
Specifications HM-6312C-9

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
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<td>+8.0V</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Applied Input or Output Voltage</td>
<td></td>
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<td>-0.3V to VCC + 0.3V</td>
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<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
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<td>-65°C to +150°C</td>
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<tr>
<td>Operating Temperature Range</td>
<td></td>
<td>-40°C to +85°C</td>
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ELECTRICAL CHARACTERISTICS  

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td></td>
<td></td>
<td>V</td>
<td>VCC = 5 ± 10%</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td></td>
<td>20% VCC</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-10</td>
<td></td>
<td>+10</td>
<td>μA</td>
<td>0V ≤ VIN ≤ VCC</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>VCC +0.1V</td>
<td></td>
<td></td>
<td>V</td>
<td>IOUT = 0</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>GND + 0.1V</td>
<td></td>
<td></td>
<td>V</td>
<td>IOUT = 0</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-10</td>
<td></td>
<td>+10</td>
<td>μA</td>
<td>0V ≤ VO ≤ VCC</td>
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<tr>
<td>ICCSB</td>
<td>Standby Supply Current</td>
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<td>500</td>
<td></td>
<td>mA</td>
<td>f = 1MHz, IO = 0</td>
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<tr>
<td>ICCOP</td>
<td>Operating Current</td>
<td>3</td>
<td></td>
<td>5</td>
<td>mA</td>
<td>V= 0 or VCC</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>5.0</td>
<td></td>
<td>7.0</td>
<td>pF</td>
<td>V= VCC or GND</td>
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<tr>
<td>CIO</td>
<td>I/O Capacitance</td>
<td>6.0</td>
<td></td>
<td>10.0</td>
<td>pF</td>
<td></td>
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D.C.

A.C.

INDUSTRIAL

<table>
<thead>
<tr>
<th>SYMBOL</th>
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<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
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<tbody>
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<td>TELQV</td>
<td>Access Time From E</td>
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<td>640 ns</td>
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<td>VCC = 5 ± 10%</td>
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<td>TGHQV</td>
<td>Output Enable Time</td>
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<td></td>
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<tr>
<td>TGLQZ</td>
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<td>390 ns</td>
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<td>Strobe Pos. Pulse Width</td>
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<td>Cycle Time</td>
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<td>940 ns</td>
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<tr>
<td>TAVEL</td>
<td>Address Set-Up Time</td>
<td></td>
<td>75 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TELAX</td>
<td>Address Hold Time</td>
<td></td>
<td>140 ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TELFV</td>
<td>Propagation to F</td>
<td></td>
<td>250 ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

(1) Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 3mA/MHz.

(2) Capacitance sampled and guaranteed - not 100% tested.

(3) A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs - 1TTL Load and 50pF.
Custom ROM Programming

HM-6312/6312A programming information is generated from the PAL III Symbolic Assembler as a “second pass” binary tape. A separate tape is required for each 1024 word ROM pattern, i.e. a separate symbolic should be generated for each 1024 word block of memory used, (0000-1777)\(^8\), (2000-3777)\(^8\), (4000-5777)\(^8\) and (6000-7777)\(^8\). A header is added to the front of each tape giving customer ID, chip select and F programming information. The header consists of 15 ASCII characters generated from a standard teletype. Channel 8 is always punched. The header begins with a rubout followed by 6 alphanumeric characters identifying the customer and the pattern number. Next are 2 characters designating true or false for inputs DX0 and DX1 to chips select gate A (see Functional Diagram), and 4 characters designating true, false, don’t care for inputs DX0, DX1, DX2 and DX3 to the RAM select gate B (see Functional Diagram). Next is one character (H or L) designating F as active high or active low. The F function is inhibited when all F inputs are VCC or don’t care (V) and F is active high. The header ends with a rubout.

### TABLE 3

<table>
<thead>
<tr>
<th>CHANNELS</th>
<th>CHARACTER</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### COMMENTS

- **SPROCKET HOLES**
  - **BEGIN HEADER**
  - 3 LETTER CUSTOMER ID
    - (A-Z, 0-9) ARE ALLOWABLE
  - 3 NUMBER CUSTOMER PATTERN NUMBER
    - (A-Z, 0-9) ARE ALLOWABLE
  - DX0 – CHIP SELECT PROGRAMMING
  - DX1 – T-TRUE, F-FALSE
  - DX0
  - DX1 – F PROGRAMMING
  - DX2 – T-TRUE, F-FALSE, V-DON’T CARE
  - DX3
  - F – IS ACTIVE LOW
  - END HEADER

- **SPROCKET HOLES**

PAL III Symbolic Assembler “second pass” output is of this form. Channel 8 only—punches indicate leader or trailer. An address is designated by a punch in channel 7. 12 bits of data are represented by two adjacent columns. DX0 – DX5 are represented by channels (6 – 1) in the first column. DX6 – 11 are represented by channels (6 – 1) in the second column.

The set location to (0200)\(^8\) is an output of the PAL III Symbolic Assembler, not otherwise needed.

The example shown above has a customer ID and pattern ISL 004. Chip selects are programmed to recognize addresses (6000-7777)\(^8\) or (3072-4095)\(^10\). RAM select is active low for addresses (0000-0377)\(^8\) or (0000-0255)\(^10\). For programs using less than 1024 words the unused locations are automatically programmed to a logic one.
Defining the address block for which $F$ is active is accomplished through programming the inputs to gate B. (See Functional Diagram). The sense of $F$ is defined by programming gate C for inverting or noninverting. These conditions are specified in the header portion of the tape, columns 9 thru 13.

Particular care is required in specifying the sense of $F$. Careful examination of the Functional Diagram reveals that $F$ actually serves two functions, 1). $F$ is anded with the inputs of gate A to enable the HM-6312 output buffers. 2). The output of $F$ is used to select RAM or other external devices, this function is always a low true.

Switching Waveforms

* $G$ has the same timing as $G$ and is inverted.

A Typical Microprocessor System

HM-6312
1024 x 12
ROM
ADDRESS SPACE
(3072 - 4095)$_{10}$

HM-6561
256 x 4
RAM

ADDRESS SPACE (0000 - 0255)$_{10}$
Features

- HM-6100 COMPATIBLE
- LOW POWER STANDBY ........................................... 1mW MAX.
- LOW POWER OPERATION ........................................ .22mW/MHz MAX.
- DATA RETENTION ................................................... @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- TWO HM-6512's CAN BE USED WITH HM-6100 AND HM-6312 WITHOUT ADDITIONAL COMPONENTS
- THREE STATE OUTPUTS
- FAST ACCESS TIME ................................................. 250nsec MAX.
- MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Description

The HM-6512 is a high speed, low power, silicon gate CMOS 768 bit static RAM organized 64 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. Inputs and three state outputs are TTL compatible. The basic part operates at 4–7 volts with a typical 5 volt, 25°C access time of 150ns.

Signal polarities and functions are specified for direct interfacing with the HM-6100 microprocessor. The device is ideally suited for minimum system all CMOS applications where low power, minimum cost, or non-volatility is required.

Functional Diagram

Pinout

18 VCC
17 MSEL
16 DX11
15 DX10
14 DX9
13 DX8
12 DX7
11 DX6
10 DX5
9 GND
8 ADR
7 DX4
6 DX3
5 DX2
4 DX1
3 DX0
2 STR
1 CS
Specifications HM-6512

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>8.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V</td>
<td>+0.3V</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HM-6512-9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military HM-6512-2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS  VCC = 5.0V ±10%, TA = Industrial or Military

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>VCC -2.0</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>-1.0</td>
<td>0.8</td>
<td></td>
<td>μA</td>
<td>0V ≤ VIN ≤ VCC</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td>+1.0</td>
<td></td>
<td>μA</td>
<td>IOH = -0.2mA</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>2.4</td>
<td></td>
<td>0.45</td>
<td>V</td>
<td>IOL = 2.0mA</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>-1.0</td>
<td>+1.0</td>
<td></td>
<td>μA</td>
<td>0V ≤ VO ≤ VCC</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICCSB</td>
<td>Supply Current Standby</td>
<td>1.0</td>
<td>100</td>
<td></td>
<td>μA</td>
<td>STR = VCC = 5.5V VIN = VCC or GND</td>
</tr>
<tr>
<td>ICCDR</td>
<td>Supply Current Data Retention</td>
<td>0.1</td>
<td>50</td>
<td></td>
<td>μA</td>
<td>STR = VCC = 3.0V VIN = VCC or GND</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>5.0</td>
<td>7.0</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>CIO</td>
<td>Input/Output Capacitance</td>
<td>6.0</td>
<td>10.0</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>TAC</td>
<td>Access Time from STR</td>
<td></td>
<td>250</td>
<td></td>
<td>ns</td>
<td>CL = 50pF See Figures 1 &amp; 2</td>
</tr>
<tr>
<td>TEN</td>
<td>Output Enable Time</td>
<td></td>
<td>200</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDIS</td>
<td>Output Disable Time</td>
<td></td>
<td>200</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TSTR</td>
<td>STR Pulse Width (Positive)</td>
<td></td>
<td>200</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TSTR</td>
<td>STR Pulse Width (Negative)</td>
<td></td>
<td>250</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TC</td>
<td>Cycle Time</td>
<td></td>
<td>450</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWP</td>
<td>Write Pulse Width (Negative)</td>
<td></td>
<td>130</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TSW</td>
<td>Address Pulse Width (Negative)</td>
<td></td>
<td>30</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TAH</td>
<td>Address Hold Time</td>
<td></td>
<td>50</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TSD</td>
<td>Data Setup Time</td>
<td></td>
<td>130</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDS</td>
<td>Data Setup Time</td>
<td></td>
<td>130</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDH</td>
<td>Data Hold Time</td>
<td></td>
<td>0</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TPS</td>
<td>MSEL Pulse Separation</td>
<td></td>
<td>150</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TMS</td>
<td>MSEL Setup Time</td>
<td></td>
<td>50</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TMH</td>
<td>MSEL Hold Time</td>
<td></td>
<td>50</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

*Guaranteed but not 100% tested.
### Specifications HM-6512C-9

**ABSOLUTE MAXIMUM RATINGS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MINIMUM</th>
<th>TYPICAL</th>
<th>MAXIMUM</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>7.0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V to VCC +0.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>Industrial HM-6512C-9</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ELECTRICAL CHARACTERISTICS**  
VCC = 5.0V ±5%, TA = Industrial

### D.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MINIMUM</th>
<th>TYPICAL</th>
<th>MAXIMUM</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical “1” Input Voltage</td>
<td>VCC -1.5</td>
<td></td>
<td></td>
<td>V</td>
<td>0V ≤ VIN ≤ VCC</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical “0” Input Voltage</td>
<td></td>
<td>0.8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-5.0</td>
<td>+5.0</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Logical “1” Output Voltage</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
<td>IOH = -0.2mA</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical “0” Output Voltage</td>
<td></td>
<td>0.45</td>
<td></td>
<td>V</td>
<td>IOL = 1.6mA</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-5.0</td>
<td>+5.0</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICCSB</td>
<td>Supply Current Standby</td>
<td></td>
<td>800</td>
<td>μA</td>
<td>STR = VCC = 5.25V</td>
<td></td>
</tr>
<tr>
<td>CIN*</td>
<td>Input Capacitance</td>
<td>5.0</td>
<td>7.0</td>
<td>pF</td>
<td>VIN = VCC or GND</td>
<td></td>
</tr>
<tr>
<td>CIO*</td>
<td>Input/Output Capacitance</td>
<td>6.0</td>
<td>10.0</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### A.C.

<table>
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<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MINIMUM</th>
<th>TYPICAL</th>
<th>MAXIMUM</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TAC</td>
<td>Access Time from STR</td>
<td></td>
<td>400</td>
<td>ns</td>
<td>CL = 50pF</td>
<td></td>
</tr>
<tr>
<td>TEN</td>
<td>Output Enable Time</td>
<td></td>
<td>300</td>
<td>ns</td>
<td>See Figures 1 &amp; 2</td>
<td></td>
</tr>
<tr>
<td>TDIS</td>
<td>Output Disable Time</td>
<td></td>
<td>300</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSTR</td>
<td>STR Pulse Width (Positive)</td>
<td></td>
<td>250</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSTR</td>
<td>STR Pulse Width (Negative)</td>
<td></td>
<td>400</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TC</td>
<td>Cycle Time</td>
<td></td>
<td>650</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TWP</td>
<td>Write Pulse Width (Negative)</td>
<td></td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TAS</td>
<td>Address Setup Time</td>
<td></td>
<td>60</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TAH</td>
<td>Address Hold Time</td>
<td></td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TDS</td>
<td>Data Setup Time</td>
<td></td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TDH</td>
<td>Data Hold Time</td>
<td></td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPS</td>
<td>MSEL Pulse Separation</td>
<td></td>
<td>150</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMS</td>
<td>MSEL Setup Time</td>
<td></td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMH</td>
<td>MSEL Hold Time</td>
<td></td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Guaranteed but not 100% tested.*
**Functional Description**

**MSEL** — The MSEL pin functions as a second chip enable and a write enable pin. If MSEL is low during the address strobe time the chip is placed in the write mode immediately. If MSEL is high during address strobe the chip performs a read operation during the first MSEL pulse and a write operation during the second MSEL pulse. In the event that a read only operation is desired the second MSEL pulse would be omitted.

**ADR** — The ADR pin provides the user with a method for using two HM-6512 chips in a HM-6100, HM-6312 ROM based system without any further decoding. The data on this pin is compared internally with address on DX5. If the two match, the chip will respond to MSEL and CS, otherwise the outputs remain high impedance and the stored data is unchanged. Using the HM-6312 with RSEL pin programmed for an active low for address 0-3778 and one or two HM-6512 RAMs provides for a 64 or 128 word scratch pad memory on page 0.

---

**Read Cycle**

---

**Truth Table**

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>STR</th>
<th>MSEL</th>
<th>DX</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H</td>
<td>X</td>
<td>Z</td>
<td>Memory Disabled</td>
</tr>
<tr>
<td>0</td>
<td>L</td>
<td>L</td>
<td>V</td>
<td>Valid, Address Latched In</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>L</td>
<td>Z</td>
<td>End of Address Time</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>H</td>
<td>V</td>
<td>Valid, Data on Output</td>
</tr>
<tr>
<td>3</td>
<td>H</td>
<td>Z</td>
<td>Z</td>
<td>End of Read Cycle</td>
</tr>
<tr>
<td>4</td>
<td>H</td>
<td>X</td>
<td>Z</td>
<td>Begin New Cycle, Same as -1</td>
</tr>
</tbody>
</table>

*Address valid during this time.

**FIGURE 1**

---

**Read Modify Write Cycle**
**TRUTH TABLE**

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>INPUTS</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H</td>
<td>Memory Disabled</td>
</tr>
<tr>
<td>0</td>
<td>( \uparrow )</td>
<td>Cycle Begins, Address Latched In</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>End of Address Time</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>Begin Read Time</td>
</tr>
<tr>
<td>3</td>
<td>L</td>
<td>End of Read Time</td>
</tr>
<tr>
<td>4</td>
<td>L</td>
<td>Begin Write Time</td>
</tr>
<tr>
<td>5</td>
<td>L</td>
<td>Data Written In</td>
</tr>
<tr>
<td>6</td>
<td>L</td>
<td>End of Write Time</td>
</tr>
<tr>
<td>7</td>
<td>H</td>
<td>End of Cycle, Memory Disabled</td>
</tr>
<tr>
<td>8</td>
<td>( \downarrow )</td>
<td>Begin New Cycle, New Address Latched In</td>
</tr>
</tbody>
</table>

*Address valid during this time.

**FIGURE 2**

**Write Cycle**

**TRUTH TABLE**

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>INPUTS</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H</td>
<td>Memory Disabled</td>
</tr>
<tr>
<td>0</td>
<td>( \uparrow )</td>
<td>Cycle Begins, Addresses are Latched</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>Write Period Begins</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>Write Completed</td>
</tr>
<tr>
<td>3</td>
<td>( \downarrow )</td>
<td>Prepare for Next Cycle</td>
</tr>
<tr>
<td>5</td>
<td>( \downarrow )</td>
<td>Cycle Ends, Next Cycle Begins</td>
</tr>
</tbody>
</table>

*Address valid during this time.

**FIGURE 3**

**Typical Microprocessor System**
Features
- HM-6100 COMPATIBLE
- LOW STANDBY POWER . 55μW MAX
- LOW OPERATING POWER . 22mW/MHz MAX
- FAST ACCESS TIME . 220nsec MAX
- DATA RETENTION VOLTAGE . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- ON CHIP ADDRESS REGISTERS
- COMMON DATA IN/OUT
- THREE STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description
The HM-6561 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM-6561 is pin for pin replaceable with the HM-6661, a 256 x 4 CMOS PROM. This allows a single memory board design with any organization of RAM and PROMs.

Functional Diagram
### Specifications HM-6561-2/HM-6561-9

#### ABSOLUTE MAXIMUM RATINGS
- **Supply Voltage** -VCC +8.0V
- **Input or Output Voltage Applied** GND -0.3V to VCC +0.3V
- **Storage Temperature** -65°C to +150°C

#### OPERATING RANGE
- **Operating Supply Voltage** -VCC
  - Military (-2) 4.5V to 5.5V
  - Industrial (-9) 4.5V to 5.5V
- **Operating Temperature**
  - Military (-2) -55°C to +125°C
  - Industrial (-9) -40°C to +85°C

#### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEMP. &amp; VCC = OPERATING RANGE</th>
<th>TEMP. = 25°C</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIN</td>
<td>MAX</td>
<td>MIN</td>
</tr>
<tr>
<td>ICCSB</td>
<td>Standby Supply Current</td>
<td>10</td>
<td>1</td>
<td>1.0</td>
</tr>
<tr>
<td>ICCOP</td>
<td>Operating Supply Current</td>
<td>4</td>
<td>1.5</td>
<td>2.5</td>
</tr>
<tr>
<td>ICCDR</td>
<td>Data Retention Supply Current</td>
<td>10</td>
<td>0.1</td>
<td>1</td>
</tr>
<tr>
<td>VCCDR</td>
<td>Data Retention Supply Voltage</td>
<td>2.0</td>
<td>2.0</td>
<td>1.4</td>
</tr>
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<td>IOL</td>
<td>Input Leakage Current</td>
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<td>+1.0</td>
<td>-0.5</td>
</tr>
<tr>
<td>IOH</td>
<td>Input/Output Leakage Current</td>
<td>-1.0</td>
<td>+1.0</td>
<td>-0.5</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
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<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>VCC-2.0</td>
<td>VCC+0.3</td>
<td>2.5</td>
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<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>0.2</td>
<td>0.35</td>
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<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>3.0</td>
<td>4.5</td>
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<td>CI</td>
<td>Input Capacitance</td>
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<td>4</td>
<td>6</td>
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<tr>
<td>CIO</td>
<td>Input/Output Capacitance</td>
<td>10</td>
<td>6</td>
<td>10</td>
</tr>
<tr>
<td>TEOV</td>
<td>Chip Enable Access Time</td>
<td>300</td>
<td>160</td>
<td>240</td>
</tr>
<tr>
<td>TAVQV</td>
<td>Address Access Time</td>
<td>300</td>
<td>150</td>
<td>240</td>
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<tr>
<td>TSLOQ</td>
<td>Chip Select Output Enable Time</td>
<td>150</td>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td>TQLQZ</td>
<td>Write Enable Output Disable Time</td>
<td>150</td>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td>TSHQZ</td>
<td>Chip Select Output Disable Time</td>
<td>150</td>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td>TELEH</td>
<td>Chip Enable Pulse Negative Width</td>
<td>300</td>
<td>240</td>
<td>160</td>
</tr>
<tr>
<td>TEHEL</td>
<td>Chip Enable Pulse Positive Width</td>
<td>100</td>
<td>70</td>
<td>50</td>
</tr>
<tr>
<td>TAVEL</td>
<td>Address Setup Time</td>
<td>0</td>
<td>0</td>
<td>-10</td>
</tr>
<tr>
<td>TELEH</td>
<td>Address Hold Time</td>
<td>50</td>
<td>40</td>
<td>30</td>
</tr>
<tr>
<td>TDVWH</td>
<td>Data Setup Time</td>
<td>150</td>
<td>120</td>
<td>100</td>
</tr>
<tr>
<td>TWHDX</td>
<td>Data Hold Time</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
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<td>TWDV</td>
<td>Write Data Delay Time</td>
<td>150</td>
<td>120</td>
<td>60</td>
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<td>TWLISH</td>
<td>Chip Select Write Pulse Setup Time</td>
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<tr>
<td>TWEH</td>
<td>Chip Enable Write Pulse Setup Time</td>
<td>300</td>
<td>240</td>
<td>160</td>
</tr>
<tr>
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<td>Chip Select Write Pulse Hold Time</td>
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<td>160</td>
</tr>
<tr>
<td>TELWH</td>
<td>Chip Enable Write Pulse Hold Time</td>
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<td>240</td>
<td>160</td>
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<td>Write Enable Pulse Width</td>
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<td>240</td>
<td>160</td>
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<td>TWLZL</td>
<td>Early Output High Z Time</td>
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<td>0</td>
<td>-10</td>
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<tr>
<td>TSHWH</td>
<td>Late Output High Z Time</td>
<td>0</td>
<td>0</td>
<td>-10</td>
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<tr>
<td>TELEL</td>
<td>Read or Write Cycle Time</td>
<td>400</td>
<td>310</td>
<td>210</td>
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**Notes:**
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.
**Specifications HM-6561-5**

### ABSOLUTE MAXIMUM RATINGS

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<tr>
<th>Parameter</th>
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<th>Max</th>
<th>Typ</th>
<th>Max</th>
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</thead>
<tbody>
<tr>
<td>Supply Voltage -VCC</td>
<td>0</td>
<td>+8.0V</td>
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</tr>
<tr>
<td>Applied Input or Output Voltage</td>
<td>GND</td>
<td>-0.3V</td>
<td>VCC</td>
<td>0.3V</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C</td>
<td>+150°C</td>
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### OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Typ</th>
<th>Max</th>
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<tbody>
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<td>Operating Supply Voltage -VCC</td>
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<td></td>
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<tr>
<td>Commercial</td>
<td>4.5V</td>
<td>5.5V</td>
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<td>Operating Temperature Commercial</td>
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<td>75°C</td>
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### ELECTRICAL CHARACTERISTICS

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<tr>
<th>SYMBOL</th>
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<th>TEMP. &amp; VCC = OPERATING RANGE</th>
<th>TEMP. = 25°C</th>
<th>VCC = 5.0V</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
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<td>ICCSB</td>
<td>Standby Supply Current</td>
<td>100</td>
<td>10</td>
<td>100</td>
<td>μA</td>
<td>IO = 0</td>
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<td>Operating Supply Current②</td>
<td>4</td>
<td>1.5</td>
<td>2.5</td>
<td>mA</td>
<td>f = 1MHz, IO = 0</td>
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<tr>
<td>VCCDR</td>
<td>Data Retention Supply Voltage</td>
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<td>2.0</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I</td>
<td>Input Leakage Current</td>
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<td>0.0</td>
<td>+0.5</td>
<td>μA</td>
<td>VCC &lt; VI &lt; GND</td>
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<tr>
<td>IIQZ</td>
<td>Input/Output Leakage Current</td>
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<td>0.0</td>
<td>+0.5</td>
<td>μA</td>
<td>GND &lt; VI &lt; VCC</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
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<td>2.0</td>
<td>1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>VCC -2.0</td>
<td>2.0</td>
<td>3.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>2.0</td>
<td>0.35</td>
<td>V</td>
<td>f = 1MHz</td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>3.0</td>
<td>4.5</td>
<td>V</td>
<td>IOH = -0.2mA</td>
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<td>6</td>
<td>pF</td>
<td></td>
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<td>Input/Output Capacitance④</td>
<td>10</td>
<td>6</td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>TEOV</td>
<td>Chip Enable Access Time</td>
<td>350</td>
<td>200</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TAVQV</td>
<td>Address Access Time</td>
<td>360</td>
<td>200</td>
<td>310</td>
<td>ns</td>
<td></td>
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<tr>
<td>TSLQX</td>
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<td>180</td>
<td>80</td>
<td>160</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWLQZ</td>
<td>Write Enable Output Disable Time</td>
<td>180</td>
<td>80</td>
<td>160</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TSHQZ</td>
<td>Chip Select Output Disable Time</td>
<td>180</td>
<td>80</td>
<td>160</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TELEH</td>
<td>Chip Enable Pulse Negative Width</td>
<td>350</td>
<td>200</td>
<td>300</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TEHEL</td>
<td>Chip Enable Pulse Positive Width</td>
<td>150</td>
<td>130</td>
<td>90</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TAVELE</td>
<td>Address Setup Time</td>
<td>10</td>
<td>10</td>
<td>0</td>
<td>ns</td>
<td></td>
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<td>Address Hold Time</td>
<td>70</td>
<td>50</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDVWH</td>
<td>Data Setup Time</td>
<td>170</td>
<td>140</td>
<td>120</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWDX</td>
<td>Data Hold Time</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWLDV</td>
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<td>200</td>
<td>170</td>
<td>60</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWLSH</td>
<td>Chip Select Write Pulse Setup Time</td>
<td>350</td>
<td>300</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWLEH</td>
<td>Chip Enable Write Pulse Setup Time</td>
<td>350</td>
<td>300</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TSLWH</td>
<td>Chip Select Write Pulse Hold Time</td>
<td>350</td>
<td>300</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TELWH</td>
<td>Chip Enable Write Pulse Hold Time</td>
<td>350</td>
<td>300</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWLWH</td>
<td>Write Enable Pulse Width</td>
<td>350</td>
<td>300</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWLSL</td>
<td>Early Output High Z Time</td>
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<td>0</td>
<td>-10</td>
<td>ns</td>
<td></td>
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<tr>
<td>TSHWH</td>
<td>Late Output High Z Time</td>
<td>0</td>
<td>0</td>
<td>-10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TELEL</td>
<td>Read or Write Cycle Time</td>
<td>500</td>
<td>430</td>
<td>290</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

① All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.

② Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.

③ Capacitance sampled and guaranteed — not 100% tested.

④ AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF. All timing measurements at 1/2 VCC.
Read Cycle

The HM-6561 Read Cycle is initiated on the falling edge of E. This signal latches the input address word into on chip registers. Minimum address setup and hold times must be met. After the required hold time, the address lines may change state without affecting device operation. In order to read the output data E, S1 and S2 must be low and W must be high. The output data will be valid at access time (TELQV).

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>INPUTS E S1 W A DO</th>
<th>OUTPUT FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H H X X Z</td>
<td>MEMORY DISABLED</td>
</tr>
<tr>
<td>0</td>
<td>X H V Z</td>
<td>CYCLE BEGINS, ADDRESSES ARE LATCHED</td>
</tr>
<tr>
<td>1</td>
<td>L L H X X</td>
<td>OUTPUT ENABLED</td>
</tr>
<tr>
<td>2</td>
<td>L L H V</td>
<td>OUTPUT VALID</td>
</tr>
<tr>
<td>3</td>
<td>L X H X V</td>
<td>OUTPUT LATCHED</td>
</tr>
<tr>
<td>4</td>
<td>H H X X Z</td>
<td>DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)</td>
</tr>
<tr>
<td>5</td>
<td>X H V Z</td>
<td>CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)</td>
</tr>
</tbody>
</table>

NOTES: 1) Device selected only if both S1 and S2 are low, and deselected if either S1 or S2 are high.

Write Cycle

The HM-6561 has output data latches that are controlled by E. On the rising edge of E the present data is latched and remains latched until E falls. Either or both S1 or S2 may be used to force the output buffers into a high impedance state.

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>INPUTS E S1 W A DO</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H H X X Z</td>
<td>MEMORY DISABLED</td>
</tr>
<tr>
<td>0</td>
<td>X X V Z</td>
<td>CYCLE BEGINS, ADDRESSES ARE LATCHED</td>
</tr>
<tr>
<td>1</td>
<td>L L L X Z</td>
<td>WRITE PERIOD BEGINS</td>
</tr>
<tr>
<td>2</td>
<td>L L X V</td>
<td>DATA IN IS WRITTEN</td>
</tr>
<tr>
<td>3</td>
<td>X H X Z</td>
<td>WRITE IS COMPLETED</td>
</tr>
<tr>
<td>4</td>
<td>H H X X Z</td>
<td>PREPARE FOR NEXT CYCLE (SAME AS -1)</td>
</tr>
<tr>
<td>5</td>
<td>X X V Z</td>
<td>CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)</td>
</tr>
</tbody>
</table>

NOTES: 1) Device selected only if both S1 and S2 are low, and deselected if either S1 or S2 are high.
In the Write Cycle the falling edge of \(E\) latches the addresses into on chip registers. The write portion of the cycle is defined as \(E, W, S1,\) and \(S2\) being low simultaneously. \(W\) may go low anytime during the cycle provided that the write enable pulse setup times (TWLEH and TWLSH) are met. The write portion of the cycle is terminated by the first rising edge of \(E, W, S1\) or \(S2\). Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the \(W\) line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the first rising edge of \(E, S1,\) or \(S2\). By positioning the write pulse at different times within the \(E\) low time (TELEH), various types of write cycles may be performed.

If the \(E\) low time (TELEH) is greater than the \(W\) pulse (TWLWH) plus an output enable time (TWHQX), a combination read-write cycle is executed.

Data may be modified an indefinite number of times during any single write cycle (TELEH).

Data multiplexing is done internal to the chip and is controlled by \(W\). When \(W\) goes low, the output buffers are forced to a high impedance state. After one output disable time (TWLOZ) input data may be applied to the bus. If it is desired that the output buffers not become active during the write cycle, \(W\) should go low with or before \(S1,\) or \(S2\) (TWLSL). It should also change to a high state after \(S1\) or \(S2\) goes high (TSHWH). Thus, TWLSL and TSHWH may be ignored unless the system design requires that the data outputs never become active during a write cycle. If the specified TWLSL time is met, the TWLDV time may be ignored. Data may then be applied to the bus whenever convenient since the output is guaranteed not to become active.
Features

- HM-6100 COMPATIBLE
- LOW STANDBY POWER ................. 55μW MAX
- LOW OPERATING POWER ............... 22mW/MHz MAX
- FAST ACCESS TIME ................. 180nsec MAX
- DATA RETENTION VOLTAGE ........... 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- TWO CHIP SELECTS FOR EASY ARRAY EXPANSION
- THREE STATE OUTPUTS
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

The HM-6518 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Functional Diagram

- All lines positive logic - active high
- Three state buffers:
  - A HIGH ➔ output active
  - L HIGH ➔ Q = D
  - G latches on rising edge of L
- Address registers and decoders:
  - Latch on rising edge of L
  - Gate on rising edge of G
### Specifications HM-6518-2/HM-6518-9

#### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage -VCC</td>
<td>-8V</td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND</td>
<td>-0.3V to VCC +0.3V</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
</tr>
</tbody>
</table>

#### OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Supply Voltage -VCC</td>
<td>4.5V to 5.5V</td>
<td></td>
</tr>
<tr>
<td>Military (-2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial (-9)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military (-2)</td>
<td>-55°C to +125°C</td>
<td></td>
</tr>
<tr>
<td>Industrial (-9)</td>
<td>-40°C to +85°C</td>
<td></td>
</tr>
</tbody>
</table>

#### ELECTRICAL CHARACTERISTICS

**D.C.**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICCSB</td>
<td>Standby Supply Current</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>ICCOP</td>
<td>Operating Supply Current</td>
<td>4</td>
<td>1.5</td>
</tr>
<tr>
<td>ICCDR</td>
<td>Data Retention Supply Current</td>
<td>10</td>
<td>1.0</td>
</tr>
<tr>
<td>VCCDR</td>
<td>Data Retention Supply Voltage</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td>II</td>
<td>Input Leakage Current</td>
<td>-1.0</td>
<td>+1.0</td>
</tr>
<tr>
<td>IOZ</td>
<td>Output Leakage Current</td>
<td>-1.0</td>
<td>+1.0</td>
</tr>
<tr>
<td>VI</td>
<td>Input Low Voltage</td>
<td>-0.3</td>
<td>0.8</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>VCC -2.0</td>
<td>VCC +0.3</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>0.2</td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>3.0</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance</td>
<td>10</td>
<td>6</td>
</tr>
</tbody>
</table>

**A.C.**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>TELQV</td>
<td>Chip Enable Access Time</td>
<td>250</td>
<td>110</td>
</tr>
<tr>
<td>TAVQV</td>
<td>Address Access Time</td>
<td>250</td>
<td>100</td>
</tr>
<tr>
<td>TSLQX</td>
<td>Chip Select Output Enable Time</td>
<td>160</td>
<td>60</td>
</tr>
<tr>
<td>TWLQX</td>
<td>Write Enable Output Disable Time</td>
<td>160</td>
<td>60</td>
</tr>
<tr>
<td>TSHQX</td>
<td>Chip Select Output Disable Time</td>
<td>160</td>
<td>60</td>
</tr>
<tr>
<td>TELHE</td>
<td>Chip Enable Pulse Negative Width</td>
<td>250</td>
<td>200</td>
</tr>
<tr>
<td>TEHEL</td>
<td>Chip Enable Pulse Positive Width</td>
<td>100</td>
<td>50</td>
</tr>
<tr>
<td>TAVEL</td>
<td>Address Setup Time</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>TELAX</td>
<td>Address Hold Time</td>
<td>50</td>
<td>40</td>
</tr>
<tr>
<td>TDVWH</td>
<td>Data Setup Time</td>
<td>110</td>
<td>80</td>
</tr>
<tr>
<td>TWHDX</td>
<td>Data Hold Time</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>TWSLH</td>
<td>Chip Select Write Pulse Setup Time</td>
<td>130</td>
<td>100</td>
</tr>
<tr>
<td>TWLEH</td>
<td>Chip Enable Write Pulse Setup Time</td>
<td>130</td>
<td>100</td>
</tr>
<tr>
<td>TSSLW</td>
<td>Chip Select Write Pulse Hold Time</td>
<td>130</td>
<td>100</td>
</tr>
<tr>
<td>TEWLH</td>
<td>Chip Enable Write Pulse Hold Time</td>
<td>130</td>
<td>100</td>
</tr>
<tr>
<td>TWLWH</td>
<td>Write Enable Pulse Width</td>
<td>130</td>
<td>100</td>
</tr>
<tr>
<td>TELEL</td>
<td>Read or Write Cycle Time</td>
<td>350</td>
<td>280</td>
</tr>
</tbody>
</table>

**NOTES:**

1. All devices tested at worst case limits. Room temp., 5 volt data provided for information - not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed - not 100% tested.
4. AC Test Conditions: Inputs - TRISE = TFALL = 20nsec; Outputs - 1 TTL load and 50pF. All timing measurements at 1/2 VCC.
## Specifications HM-6518-5

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>-8.0V</td>
<td>+8.0V</td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V</td>
<td>VCC +0.3V</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
</tr>
</tbody>
</table>

### OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Supply Voltage</td>
<td>4.5V</td>
<td>5.5V</td>
</tr>
<tr>
<td>Commercial</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>0°C to 75°C</td>
<td></td>
</tr>
<tr>
<td>Commercial</td>
<td></td>
<td></td>
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</tbody>
</table>

### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>TEMP. &amp; VCC = 0V</th>
<th>TEMP. &amp; VCC = 5.0V</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICCSB</td>
<td>Standby Supply Current</td>
<td>100</td>
<td>100</td>
<td>10</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td>ICCOP</td>
<td>Operating Supply Current</td>
<td>4</td>
<td>4</td>
<td>1.5</td>
<td>2.5</td>
<td>mA</td>
</tr>
<tr>
<td>VCCDR</td>
<td>Data Retention Supply Voltage</td>
<td>2.0</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IIN</td>
<td>Input Leakage Current</td>
<td>-1.0</td>
<td>+1.0</td>
<td>-0.5</td>
<td>+0.5</td>
<td>µA</td>
</tr>
<tr>
<td>IOZ</td>
<td>Output Leakage Current</td>
<td>-1.0</td>
<td>+1.0</td>
<td>-0.5</td>
<td>+0.5</td>
<td>µA</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>-0.3</td>
<td>0.8</td>
<td>-0.3</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>VCC -2.0</td>
<td>VCC +0.3</td>
<td>2.5</td>
<td>2.0</td>
<td>5.3</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>0.4</td>
<td>0.2</td>
<td>0.35</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>2.4</td>
<td>3.0</td>
<td>4.5</td>
<td>V</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>pF</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

### AC Test Conditions:
- Inputs – TRISE = TFALL = 20nsec
- Outputs – 1 TTL load and 50pF
- All timing measurements at 1/2 VCC.
Read Cycle

TRUTH TABLE

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>INPUTS E S W A D Q</th>
<th>OUTPUT Q</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H H X X X Z</td>
<td>Z</td>
<td>MEMORY DISABLED</td>
</tr>
<tr>
<td>0</td>
<td>X X H V Z</td>
<td>Z</td>
<td>CYCLE BEGINS, ADDRESSES ARE LATCHED</td>
</tr>
<tr>
<td>1</td>
<td>L L H X X</td>
<td>V</td>
<td>OUTPUT ENABLED</td>
</tr>
<tr>
<td>2</td>
<td>L L H X X</td>
<td>V</td>
<td>OUTPUT LATCHED</td>
</tr>
<tr>
<td>3</td>
<td>L L H X X</td>
<td>V</td>
<td>OUTPUT LATCHED</td>
</tr>
<tr>
<td>4</td>
<td>H H X X Z</td>
<td>Z</td>
<td>DEVICE DISABLED, PREPARE FOR NEXT CYCLE (SAME AS -1)</td>
</tr>
<tr>
<td>5</td>
<td>X X H V X</td>
<td>Z</td>
<td>CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)</td>
</tr>
</tbody>
</table>

NOTES: Device selected only if both $S_1$ and $S_2$ are low, and deselected if either $S_1$ or $S_2$ are high.

In the HM-6518 read cycle the address information is latched into the on chip registers on the falling edge of $E$ ($T = 0$). Minimum address setup and hold time requirements must be met. After the required hold time the addresses may change state without affecting device operation. In order for the output to be read $S_1$, $S_2$, and $E$ must be low, $W$ must be high. When $E$ goes high the output data is latched into an on chip register. Taking either or both $S_1$ or $S_2$ high forces the output buffer to a high impedance state. The output data may be re-enabled at any time by taking $S_1$ and $S_2$ low. On the falling edge of $E$ the data will be unlatched.

Write Cycle

TRUTH TABLE

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>INPUTS E W S A D Q</th>
<th>OUTPUT Q</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H X X Z X</td>
<td>Z</td>
<td>MEMORY DISABLED</td>
</tr>
<tr>
<td>0</td>
<td>X X V Z</td>
<td>Z</td>
<td>CYCLE BEGINS, ADDRESSES ARE LATCHED</td>
</tr>
<tr>
<td>1</td>
<td>L L X X V</td>
<td>Z</td>
<td>WRITE MODE HAS BEGUN</td>
</tr>
<tr>
<td>2</td>
<td>L L X X V</td>
<td>Z</td>
<td>DATA IS WRITTEN</td>
</tr>
<tr>
<td>3</td>
<td>X X X X Z</td>
<td>Z</td>
<td>WRITE COMPLETED</td>
</tr>
<tr>
<td>4</td>
<td>H X X Z</td>
<td>Z</td>
<td>PREPARE FOR NEXT CYCLE (SAME AS -1)</td>
</tr>
<tr>
<td>5</td>
<td>X X V X</td>
<td>Z</td>
<td>CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)</td>
</tr>
</tbody>
</table>

NOTES: Device selected only if both $S_1$ and $S_2$ are low, and deselected if either $S_1$ or $S_2$ are high.
The write cycle is initiated by the falling edge of $E$ which latches the address information into the on chip registers. The write portion of the cycle is defined as $E, W, S1$, and $S2$ being low simultaneously. $W$ may go low anytime during the cycle provided that the write enable pulse set-up time (TWLEH) is met. The write portion of the cycle is terminated by the first rising edge of either $E, W, S1$ or $S2$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $W$ line may remain low until all desired locations have been written. When this method is used data setup and hold times must be referenced to the rising edge of $E$. By positioning the $W$ pulse at different times within the $E$ low time (TELEH), various types of write cycles may be performed.

If the $E$ low time (TELEH) is greater than the $W$ pulse (TWLWH) plus an output enable time (TSLOX), a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

The data input and data output pins may be tied together for use with a common I/O data bus structure. When using the RAM in this method allow a minimum of one output disable time (TWLOZ) after $W$ goes low before applying input data to the bus. This will insure that the output buffers are not active.
Features

- HM-6100 COMPATIBLE
- LOW POWER STANDBY ........................................... 1mW
- LOW POWER OPERATION ......................................... 35mW/MHz MAX
- DATA RETENTION @ 2.0 VOLTS.
- TTL COMPATIBLE INPUT/OUTPUT.
- "THREE STATE" OUTPUT.
- SEPARATE CHIP SELECT FOR EASE OF MEMORY EXPANSION.
- FULL MILITARY AND INDUSTRIAL TEMPERATURE RANGES.
- ON CHIP ADDRESS REGISTER.

Description

The HM-6533 is a 1024 x 4 clocked static CMOS RAM designed specifically to interface with the HM-6100 Microprocessor. The device is manufactured utilizing self-aligned silicon gate technology. Extremely low power drain makes the HM-6533 an ideal candidate for battery powered systems.

On chip latching address registers and "Three State" I/O buffers enable the HM-6533 to operate in a multiplexed bus system with a minimum of support circuitry. Separate chip select and output disable pins allow for easy expansion. The output buffers can be disabled by the G, G, or S pins (see Truth Table).

Wide supply voltage range and high noise immunity offer the system designer a large degree of flexibility. Data retention is guaranteed down to 2.0V VCC making non-volatile memory systems simple to implement.

Functional Diagram

Pinout

<table>
<thead>
<tr>
<th>Pinout</th>
<th>Top View</th>
</tr>
</thead>
<tbody>
<tr>
<td>A6</td>
<td>VCC</td>
</tr>
<tr>
<td>A7</td>
<td>A0</td>
</tr>
<tr>
<td>A8</td>
<td>A1</td>
</tr>
<tr>
<td>A9</td>
<td>A2</td>
</tr>
<tr>
<td>DQ0</td>
<td>A3</td>
</tr>
<tr>
<td>DQ1</td>
<td>A4</td>
</tr>
<tr>
<td>DQ2</td>
<td>A5</td>
</tr>
<tr>
<td>DQ3</td>
<td>A6</td>
</tr>
<tr>
<td>NC</td>
<td>A7</td>
</tr>
<tr>
<td>T</td>
<td>A8</td>
</tr>
<tr>
<td>S</td>
<td>A9</td>
</tr>
<tr>
<td>NC</td>
<td>E</td>
</tr>
<tr>
<td>NC</td>
<td>G</td>
</tr>
</tbody>
</table>

Logic Symbol

 PIN NAMES
A Address Input
E Chip Enable
W Write Enable
DQ Data In/Out
S Chip Select
G Output Enable

Functional Diagram
### Specifications HM-6533-2/HM-6533-9

#### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Min TYP</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage - VCC</td>
<td>±8.0V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Applied Input or Output Voltage</td>
<td>GND-0.3V</td>
<td>VCC+0.3V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### OPERATING RANGE

- Operating Supply Voltage - VCC: 4.5V to 5.5V
- Operating Temperature Range:
  - Military (-2): -55°C to +125°C
  - Industrial (-9): -40°C to +85°C

#### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>25°C</th>
<th>5.0V (1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICCSB</td>
<td>Standby Supply Current</td>
<td>100</td>
<td>0.1</td>
</tr>
<tr>
<td>ICCOP</td>
<td>Operating Current</td>
<td>8</td>
<td>6</td>
</tr>
<tr>
<td>ICCDR</td>
<td>Data Retention Supply Current</td>
<td>50</td>
<td>1.0</td>
</tr>
<tr>
<td>VCCDR</td>
<td>Data Retention Supply Voltage</td>
<td>2.0</td>
<td>2.0</td>
</tr>
<tr>
<td>II</td>
<td>Input Leakage Current</td>
<td>-1.0</td>
<td>+1.0</td>
</tr>
<tr>
<td>IOZ</td>
<td>Output Leakage Current</td>
<td>-1.0</td>
<td>+1.0</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>-0.3</td>
<td>0.8</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>VCC-2.0</td>
<td>VCC+0.3</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>0.2</td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>3.0</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>CIO</td>
<td>Output Capacitance</td>
<td>10</td>
<td>6</td>
</tr>
<tr>
<td>TELOV</td>
<td>Chip Enable Access Time</td>
<td>400</td>
<td>300</td>
</tr>
<tr>
<td>TSLQX</td>
<td>Chip Select Output Enable Time</td>
<td>200</td>
<td>110</td>
</tr>
<tr>
<td>TSHQZ</td>
<td>Chip Select Output Disable Time</td>
<td>200</td>
<td>110</td>
</tr>
<tr>
<td>TGLQX</td>
<td>Output Enable Time</td>
<td>200</td>
<td>110</td>
</tr>
<tr>
<td>TGHQX</td>
<td>Output Disable Time</td>
<td>200</td>
<td>110</td>
</tr>
<tr>
<td>TELEL</td>
<td>Read or Write Cycle Time</td>
<td>600</td>
<td>475</td>
</tr>
<tr>
<td>TEHEL</td>
<td>Chip Enable Positive Pulse Width</td>
<td>200</td>
<td>175</td>
</tr>
<tr>
<td>TELEH</td>
<td>Chip Enable Negative Pulse Width</td>
<td>400</td>
<td>350</td>
</tr>
<tr>
<td>TAVEL</td>
<td>Address Setup Time</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>TELAX</td>
<td>Address Hold Time</td>
<td>75</td>
<td>75</td>
</tr>
<tr>
<td>TWLWH</td>
<td>Write Enable Pulse Width</td>
<td>220</td>
<td>130</td>
</tr>
<tr>
<td>TWLEH</td>
<td>Write Enable Pulse Setup Time</td>
<td>220</td>
<td>130</td>
</tr>
<tr>
<td>TELWH</td>
<td>Chip Enable Write Pulse Hold Time</td>
<td>220</td>
<td>130</td>
</tr>
<tr>
<td>TWLWH</td>
<td>Chip Select Write Pulse Setup Time</td>
<td>220</td>
<td>130</td>
</tr>
<tr>
<td>TLWH</td>
<td>Chip Select Write Pulse Hold Time</td>
<td>220</td>
<td>130</td>
</tr>
<tr>
<td>TDVWH</td>
<td>Data Setup Time</td>
<td>130</td>
<td>100</td>
</tr>
<tr>
<td>TWHDX</td>
<td>Data Hold Time</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>TDVSH</td>
<td>Data to Chip Select Setup Time</td>
<td>130</td>
<td>100</td>
</tr>
<tr>
<td>TSHDX</td>
<td>Data to Chip Select Hold Time</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>TSLSH</td>
<td>Chip Select Write Pulse Hold Time</td>
<td>130</td>
<td>100</td>
</tr>
</tbody>
</table>

#### NOTES:

1. All devices tested at worst case limits. Room temperature, 5V data provided for information – not guaranteed.
2. Operating supply current (ICCP) is proportional to operating frequency. Example: Typical ICCP = 6mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – Trise = Tfall = 20ns.

Outputs – 1 TTL Load and 50pF.
### Specifications HM-6533C-9

#### ABSOLUTE MAXIMUM RATINGS
- Supply Voltage-VCC: $\pm 8.0V$
- Applied Input or Output Voltage: GND to $VCC + 0.3V$
- Storage Temperature Range: $-65^\circ C$ to $+150^\circ C$

#### OPERATING RANGE
- Operating Supply Voltage-VCC: 4.5V to 5.5V
- Operating Temperature Range: $-40^\circ C$ to $+85^\circ C$

#### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>VCC &amp; TEMP = OPERATING RANGE</th>
<th>TEMP = 25$^\circ$C VCC = 5.0V (1)</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICCSB</td>
<td>Standby Supply Current</td>
<td>1.0</td>
<td>0.1</td>
<td>1.0 mA</td>
</tr>
<tr>
<td>ICCOP</td>
<td>Operating Current</td>
<td>8</td>
<td>6</td>
<td>$+7 \mu A$</td>
</tr>
<tr>
<td>II</td>
<td>Input Leakage Current</td>
<td>-10</td>
<td>$+7 \mu A$</td>
<td>GND &lt; V1 &lt; VCC</td>
</tr>
<tr>
<td>IOZ</td>
<td>Output Leakage Current</td>
<td>-10</td>
<td>$+7 \mu A$</td>
<td>GND &lt; V0 &lt; VCC</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>-0.8</td>
<td>2.0</td>
<td>1.5 V</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>VCC - 2.0</td>
<td>VCC + 0.3</td>
<td>2.5</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>0.2</td>
<td>0.35 V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>3.0</td>
<td>4.5 V</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>6</td>
<td>4</td>
<td>6 pF</td>
</tr>
<tr>
<td>CIO</td>
<td>Output Capacitance</td>
<td>10</td>
<td>6</td>
<td>10 pF</td>
</tr>
<tr>
<td>CQ</td>
<td>Input Capacitance</td>
<td>2.0</td>
<td>2.0</td>
<td>5.3 V</td>
</tr>
<tr>
<td>CQ</td>
<td>Output Capacitance</td>
<td>10</td>
<td>6</td>
<td>10 pF</td>
</tr>
</tbody>
</table>

#### NOTES:
1. All devices tested at worst case limits. Room temperature, 5V data provided for information - not guaranteed.
2. Operating supply current (ICCOP) is proportional to operating frequency. Example: Typical ICCOP = 6mA/MHz.
3. Capacitance sampled and guaranteed - not 100% tested.
4. AC test conditions: Inputs - $Trise = Tfall = 20\, ns$,
   Outputs - 1 TTL Load and 50pF.
The read cycle is initiated by the falling edge of \( \bar{E} \). This signal latches the input address word into on chip registers providing that minimum address setup and hold times are met. After the required hold time, the address inputs may change state without affecting device operation. For the output to be read, \( \bar{G} \) and \( \bar{E} \) and \( \bar{S} \) must be low; \( W \) must be high. The output data will be valid at access time (TELOV) or at one output enable time (TSHQX or TGLOX), whichever is the latter occurring signal.

\( G \) and \( \bar{G} \) are complementary signals which simplify the external logic required for decoding in expanded memory arrays. Either or both of these signals may be used to disable the outputs when tying several memories in an array. The HM-6533 has output data latches that are controlled by \( \bar{E} \).

When \( \bar{E} \) goes high the outputs are latched to contain the present data. The output buffers can be forced to a high impedance state by either \( \bar{G} \) or \( \bar{S} \) but the latches will only unlatch on the falling edge of \( \bar{E} \).

---

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>INPUTS</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( E )</td>
<td>( \bar{E} )</td>
</tr>
<tr>
<td></td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>0</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>3</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>4</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>5</td>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>
As in the read mode, the write cycle is initiated by the falling edge of $\bar{E}$ which latches the addresses. The write portion of the cycle is defined as $E$ and $W$ being low simultaneously with $\bar{S}$ low. Since the inputs and outputs are tied together, $G$ must be low. The write portion of the cycle is terminated on the first rising edge of $E$, $W$, or $S$. Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the $W$ line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of $E$ or $\bar{S}$, whichever occurs first. By positioning the $W$ pulse at different times within the $\bar{E}$ low time (TELEH) various types of write cycles may be performed.

If the $\bar{E}$ low time (TELEH) is greater than the $W$ pulse (TWLWH) plus an output enable time (TSHQX or TGHQX) a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).
HM-6100 COMPATIBLE READ WRITE CYCLE

HM-6100 C LOCK

HM-6100 STATE TIME

(TXMAR)

(DX BUS)

VALID ADD
(MEMSEL)

Te EHEL

DON'T CARE READ

WRITE DATA

NEW ADD

TSHQZ

TDVSH

Y

(XTC)

TIME REFERENCE

-1 0 1 2 3 4 5 6

TRUTH TABLE

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>E</th>
<th>S</th>
<th>W</th>
<th>G</th>
<th>G</th>
<th>A</th>
<th>DQ</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>Z</td>
<td>Memory Disabled</td>
</tr>
<tr>
<td>0</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>V</td>
<td>Z</td>
<td>Cycle begins Addresses are Latched</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>V</td>
<td>Memory Output Enabled</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>Z</td>
<td>Memory Output Disabled</td>
</tr>
<tr>
<td>3</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>V</td>
<td>Valid Input Data present preparing to Write</td>
</tr>
<tr>
<td>4</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>V</td>
<td>New Data Written In</td>
</tr>
<tr>
<td>5</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>Z</td>
<td>Prepare for next cycle (Same as -1)</td>
</tr>
<tr>
<td>6</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>V</td>
<td>Z</td>
<td>Z</td>
<td>Cycle ends, next cycle begins (Same as 0)</td>
</tr>
</tbody>
</table>

HM-6100 1K x 12 MEMORY SYSTEM USING 3 HM-6533 RAMS
Features

- HM-6100 COMPATIBLE
- LOW POWER STANDBY .............. 1mW MAX
- LOW POWER OPERATION .................. 35mW/MHz MAX
- DATA RETENTION .................. @ 2.0 VOLTS
- TTL COMPATIBLE INPUT/OUTPUT
- THREE STATE OUTPUT
- SEPARATE CHIP SELECT FOR EASE OF MEMORY EXPANSION
- FULL MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- ON CHIP ADDRESS REGISTER

Description

The HM-6543 is a 4096 x 1 static CMOS RAM fabricated with self-aligned silicon gate technology. The device is designed to interface directly with the HM-6100, 12 bit Microprocessor.

On chip latches are provided for addresses and output data. The chip provides a three state output buffer for ease of use on a common bus.

The HM-6543 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention, supply voltage and supply current are guaranteed over temperature.

Functional Diagram
## Specifications HM-6543-2/HM-6543-9

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage ~VCC</td>
<td>100</td>
<td>200</td>
</tr>
<tr>
<td>Applied Input or Output Voltage</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>50</td>
<td>10</td>
</tr>
</tbody>
</table>

### OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Supply Voltage ~VCC</td>
<td>4.5</td>
<td>5.5</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-55°C to +125°C</td>
<td></td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEMP. &amp; VCC = OPERATING RANGE</th>
<th>TEMP. = 25°C</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min</td>
<td>Max</td>
<td>TYP</td>
<td>Max</td>
</tr>
<tr>
<td>ICBS</td>
<td>Standby Supply Current</td>
<td>100</td>
<td>2</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>ICOP</td>
<td>Operating Current</td>
<td>8</td>
<td>6</td>
<td>7</td>
<td>mA</td>
</tr>
<tr>
<td>ICDDR</td>
<td>Data Retention Supply Current</td>
<td>50</td>
<td>1</td>
<td>5</td>
<td>μA</td>
</tr>
<tr>
<td>VCCDR</td>
<td>Data Retention Supply Voltage</td>
<td>2.0</td>
<td>1.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>IL</td>
<td>Input Leakage Current</td>
<td>-1.0</td>
<td>+1.0</td>
<td>0.0</td>
<td>+0.5</td>
</tr>
<tr>
<td>IOZ</td>
<td>Output Leakage Current</td>
<td>-1.0</td>
<td>+1.0</td>
<td>0.0</td>
<td>+0.5</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>-0.3</td>
<td>0.8</td>
<td>-0.3</td>
<td>2.0</td>
</tr>
<tr>
<td>VIL</td>
<td>Input High Voltage</td>
<td>VCC</td>
<td>VCC</td>
<td>2.5</td>
<td>2.0</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td>0.2</td>
<td>0.35</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>3.0</td>
<td>4.5</td>
<td></td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>pF</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance</td>
<td>10</td>
<td>10</td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

### NOTES:

1. All devices tested at worst case limits. Room temp., 5 volt data provided — not guaranteed.
2. Operating Supply Current (ICOP) is proportional to Operating Frequency. Example: Typical ICOP = 6mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. A.C. Test Conditions: Inputs — TRISE = TFALL = 20ns; Outputs — 1 TTL load and 50pF.

A.C. Test Conditions: Inputs — TRISE = TFALL = 20ns; Outputs — 1 TTL load and 50pF.
### Specifications HM-6543C-9

#### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>-8.0V</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Applied Input or Output Voltage</td>
<td>GND -0.3V to VCC +0.3V</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
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<td></td>
<td></td>
<td></td>
<td></td>
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</table>

#### OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Supply Voltage</td>
<td>4.5V to 5.5V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEMP. &amp; VCC = OPERATING RANGE</th>
<th>TEMP. = 25°C</th>
<th>VCC = 5.0V</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
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<tbody>
<tr>
<td>ICCSB</td>
<td>Standby Supply Current</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td></td>
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<td>1.0</td>
<td>0.1</td>
<td>0.1</td>
<td>1.0</td>
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<tr>
<td>ICCOP</td>
<td>Operating Current</td>
<td>8</td>
<td></td>
<td>6</td>
<td></td>
<td>7</td>
</tr>
<tr>
<td>II</td>
<td>Input Leakage Current</td>
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<td>+10</td>
<td>-7</td>
<td>+0.5</td>
<td>+7</td>
</tr>
<tr>
<td>IOZ</td>
<td>Output Leakage Current</td>
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<td>+10</td>
<td>-7</td>
<td>+0.5</td>
<td>+7</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>-0.3</td>
<td>0.8</td>
<td>-0.3</td>
<td>2.0</td>
<td>1.5</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>VCC -2.0</td>
<td>VCC +3.0</td>
<td>2.5</td>
<td>2.0</td>
<td>5.3</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>0.4</td>
<td></td>
<td>0.2</td>
<td></td>
<td>0.35</td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td></td>
<td>3.0</td>
<td></td>
<td>4.5</td>
</tr>
<tr>
<td>CI</td>
<td>Input Capacitance</td>
<td>6</td>
<td></td>
<td>4</td>
<td></td>
<td>6</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance</td>
<td>10</td>
<td></td>
<td>6</td>
<td></td>
<td>10</td>
</tr>
</tbody>
</table>

**A.C.**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>TEMP. &amp; VCC = OPERATING RANGE</th>
<th>TEMP. = 25°C</th>
<th>VCC = 5.0V</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
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</thead>
<tbody>
<tr>
<td>TELQV</td>
<td>Chip Enable Access Time</td>
<td>450</td>
<td>350</td>
<td>400</td>
<td>400</td>
<td>ns</td>
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<tr>
<td>TSLOX</td>
<td>Chip Select Output Enable Time</td>
<td>300</td>
<td>130</td>
<td>180</td>
<td>180</td>
<td>ns</td>
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<tr>
<td>TSHQZ</td>
<td>Chip Select Output Disable Time</td>
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<td>130</td>
<td>180</td>
<td>180</td>
<td>ns</td>
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<tr>
<td>TGLOX</td>
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<td>130</td>
<td>180</td>
<td>180</td>
<td>ns</td>
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<td>TGHQZ</td>
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<td>130</td>
<td>180</td>
<td>180</td>
<td>ns</td>
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<tr>
<td>TELEN</td>
<td>Read or Write Cycle Time</td>
<td>700</td>
<td>560</td>
<td>650</td>
<td>650</td>
<td>ns</td>
</tr>
<tr>
<td>TEHEL</td>
<td>Chip Enable Positive Pulse Width</td>
<td>250</td>
<td>210</td>
<td>250</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>TELEH</td>
<td>Chip Enable Negative Pulse Width</td>
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<td>350</td>
<td>400</td>
<td>400</td>
<td>ns</td>
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<td>Address Setup Time</td>
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<td>30</td>
<td>50</td>
<td>50</td>
<td>ns</td>
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<tr>
<td>TELAX</td>
<td>Address Hold Time</td>
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<td>75</td>
<td>100</td>
<td>100</td>
<td>ns</td>
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<td>TWLWH</td>
<td>Write Enable Pulse Width</td>
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<td>175</td>
<td>200</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>TWLEH</td>
<td>Write Enable Pulse Setup Time</td>
<td>300</td>
<td>175</td>
<td>200</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>TELWH</td>
<td>Chip Enable Write Pulse Hold Time</td>
<td>300</td>
<td>175</td>
<td>200</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>TWSLH</td>
<td>Chip Select Write Pulse Setup Time</td>
<td>300</td>
<td>175</td>
<td>200</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>TSLWH</td>
<td>Chip Select Write Pulse Hold Time</td>
<td>300</td>
<td>175</td>
<td>200</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>TDVWH</td>
<td>Data Setup Time</td>
<td>200</td>
<td>120</td>
<td>150</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>TWHDX</td>
<td>Data Hold Time</td>
<td>75</td>
<td>25</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>TDVSH</td>
<td>Data To Chip Select Setup Time</td>
<td>220</td>
<td>120</td>
<td>150</td>
<td>150</td>
<td>ns</td>
</tr>
<tr>
<td>TSHDX</td>
<td>Data to Chip Select Hold Time</td>
<td>75</td>
<td>25</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>TSLSH</td>
<td>Chip Select Write Setup Time</td>
<td>300</td>
<td>175</td>
<td>200</td>
<td>200</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTES:**

1. All devices tested at worst case limits. Room temp., 5 volt data provided — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example Typical ICCOP = 6mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. A.C. Test Conditions: Inputs — TRISE = TFALL = 20ns; Outputs — 1TTL load and 50pF.
Read Cycle

TRUTH TABLE

<table>
<thead>
<tr>
<th>TIME</th>
<th>INPUTS</th>
<th>OUTPUT</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H</td>
<td>H</td>
<td>Z</td>
</tr>
<tr>
<td>0</td>
<td>H</td>
<td>H</td>
<td>Z</td>
</tr>
<tr>
<td>1</td>
<td>L</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>2</td>
<td>L</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>3</td>
<td>L</td>
<td>L</td>
<td>V</td>
</tr>
<tr>
<td>4</td>
<td>H</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>5</td>
<td>H</td>
<td>H</td>
<td>V</td>
</tr>
</tbody>
</table>

The read cycle is initiated by the falling edge of \( \bar{E} \). This signal latches the input address word into on chip registers providing that minimum address setup and hold times are met. After the required hold time, the address inputs may change state without affecting device operation. For the output to be read, \( G^* \) and \( E \) and \( S \) must be low; \( W \) must be high. The output data will be valid at access time (TELQV) or at one output enable time (TSLOX or TGLOX), whichever is the later occurring signal.

\( G \) and \( G^* \) are complementary signals which simplify the external logic required for decoding in expanded memory arrays. Either or both of these signals may be used to disable the outputs when or-tying several memories in an array. The HM-6543 has an output data latch that is controlled by \( \bar{E} \).

When \( \bar{E} \) goes high the outputs are latched to contain the present data. The output buffers can be forced to a high impedance state by either \( G \) or \( S \) but the latch will only unlatch on the falling edge of \( \bar{E} \).

Write Cycle
TRUTH TABLE

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>INPUTS</th>
<th>OUTPUT</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H H X X X X X</td>
<td>Z</td>
<td>MEMORY DISABLED</td>
</tr>
<tr>
<td>0</td>
<td>\lor X X X V X</td>
<td>Z</td>
<td>CYCLE BEGINS, ADDRESSES ARE LATCHED</td>
</tr>
<tr>
<td>1</td>
<td>L L X \lor X V</td>
<td>Z</td>
<td>WRITE PERIOD BEGINS</td>
</tr>
<tr>
<td>2</td>
<td>L L X X X X</td>
<td>Z</td>
<td>DATA IN IS WRITTEN</td>
</tr>
<tr>
<td>3</td>
<td>\lor X X H X X</td>
<td>Z</td>
<td>WRITE IS COMPLETED</td>
</tr>
<tr>
<td>4</td>
<td>H H X X X X</td>
<td>Z</td>
<td>PREPARE FOR NEXT CYCLE (SAME AS -1)</td>
</tr>
<tr>
<td>5</td>
<td>\lor X X X V X</td>
<td>Z</td>
<td>CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)</td>
</tr>
</tbody>
</table>

As in the read mode, the write cycle is initiated by the falling edge of \( E \) which latches the addresses. The write portion of the cycle is defined as \( E \) and \( W \) being low simultaneously with \( S \) low.

The write portion of the cycle is terminated on the first rising edge of \( E \), \( W \), or \( S \). Data setup and hold times must be referenced to the terminating signal.

If a series of consecutive write cycles are to be performed, the \( W \) line may remain low until all desired locations have been written. When this method is used, data setup and hold times must be referenced to the rising edge of \( E \) or \( S \), whichever occurs first. By positioning the \( W \) pulse at different times within the \( E \) low time (TELEH) various types of write cycles may be performed.

If the \( E \) low time (TELEH) is greater than the \( W \) pulse (TWLWH) plus an output enable time (TSLOX or TGLOX) a combination read-write cycle is executed. Data may be modified an indefinite number of times during any write cycle (TELEH).

COMMON I/O OPERATION

The HM-6543 is readily adaptable for use in a common I/O bus oriented system. In this mode of operation the \( G \) or \( \overline{G} \) pins are used to disable the output before the input data is presented on the bus. When the chip is deselected (\( S \) high) the output is forced to the high impedance state thereby leaving the bus free to be driven from another source.

HM-6100 Compatible Read Write Cycle

<table>
<thead>
<tr>
<th>TIME REFERENCE</th>
<th>INPUTS</th>
<th>OUTPUT</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1</td>
<td>H H H L X L X X</td>
<td>Z</td>
<td>MEMORY DISABLED</td>
</tr>
<tr>
<td>0</td>
<td>\lor H H H L V X</td>
<td>Z</td>
<td>CYCLE BEGINS, ADDRESSES ARE LATCHED</td>
</tr>
<tr>
<td>1</td>
<td>L L H H L X X</td>
<td>X</td>
<td>MEMORY OUTPUT ENABLED</td>
</tr>
<tr>
<td>2</td>
<td>L H H H L X X</td>
<td>Z</td>
<td>MEMORY OUTPUT DISABLED</td>
</tr>
<tr>
<td>3</td>
<td>L L L L L X V</td>
<td>Z</td>
<td>VALID INPUT DATA PRESENT PREPARING TO WRITE</td>
</tr>
<tr>
<td>4</td>
<td>L \lor L L L X V</td>
<td>Z</td>
<td>NEW DATA WRITTEN IN</td>
</tr>
<tr>
<td>5</td>
<td>\lor H L H X X X</td>
<td>Z</td>
<td>PREPARE FOR NEXT CYCLE (SAME AS -1)</td>
</tr>
<tr>
<td>6</td>
<td>H H H L V X X</td>
<td>Z</td>
<td>CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)</td>
</tr>
<tr>
<td>CMOS Bus Driver Family Pinouts</td>
<td>4—2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Serial Interface</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-4702/6405 Programmable</td>
<td>4—4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bit Rate Generator</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-6402 Universal Asynchronous</td>
<td>4—10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Receiver/Transmitter (UART)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-6408 Asynchronous Serial</td>
<td>4—15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Manchester Adapter (ASMA)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMOS Bus Drivers</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-6431 Hex Latched Bus</td>
<td>4—20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Driver</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-6432 Hex Bi-Directional</td>
<td>4—24</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bus Driver</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-6433 Quad Bus Separator/</td>
<td>4—28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Driver</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-6434 Octal Resettable</td>
<td>4—32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Latched Bus Driver</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-6435 Hex Resettable</td>
<td>4—35</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Latched Bus Driver</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-6436 Octal Bus Buffer/</td>
<td>4—38</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Driver</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-6440 One-of-Eight Latched</td>
<td>4—41</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Decoder/Driver</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HD-6495 Hex Bus Buffer/Driver</td>
<td>4—45</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
CMOS Bus Driver Family

HD-6431 CMOS HEX LATCHING BUS DRIVER

FEATURES
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY .... 300pF
- SOURCE CURRENT .... 4mA
- SINK CURRENT ....... 6mA
- PROPAGATION DELAY: 65nsec @ 5V

TRUTH TABLE

<table>
<thead>
<tr>
<th>CONTROL INPUTS</th>
<th>DATA PORT STATUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>E L A Y</td>
<td></td>
</tr>
<tr>
<td>H L X H I-Z</td>
<td></td>
</tr>
<tr>
<td>H H X H I-Z</td>
<td></td>
</tr>
<tr>
<td>L I X *</td>
<td></td>
</tr>
<tr>
<td>L H L L L L</td>
<td></td>
</tr>
<tr>
<td>L H H H H H</td>
<td></td>
</tr>
</tbody>
</table>

* Data is latched to the value of the last input
X = Don't Care
H-I-Z = High Impedance
I = Transition from High to Low Level

HD-6432 CMOS HEX BI-DIRECTIONAL BUS DRIVER

FEATURES
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY .... 300pF
- SOURCE CURRENT .... 4mA
- SINK CURRENT ....... 6mA
- PROPAGATION DELAY: 45nsec @ 5V

TRUTH TABLE

<table>
<thead>
<tr>
<th>CONTROL INPUTS</th>
<th>DATA PORT STATUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>E A B A B A B</td>
<td>A B</td>
</tr>
<tr>
<td>L X H L D I</td>
<td></td>
</tr>
<tr>
<td>X H H L D I</td>
<td></td>
</tr>
<tr>
<td>H L X H I O</td>
<td></td>
</tr>
<tr>
<td>L L L X D O I</td>
<td></td>
</tr>
<tr>
<td>L X L X ISOLATED</td>
<td></td>
</tr>
<tr>
<td>X H X H ISOLATED</td>
<td></td>
</tr>
<tr>
<td>L X X H ISOLATED</td>
<td></td>
</tr>
<tr>
<td>X H L X ISOLATED</td>
<td></td>
</tr>
<tr>
<td>NOT ALLOWED</td>
<td></td>
</tr>
</tbody>
</table>

I = Input, O = Output, X = Don't Care

HD-6433 CMOS QUAD BUS SEPARATOR/DRIVER

FEATURES
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY .... 300pF
- SOURCE CURRENT .... 4mA
- SINK CURRENT ....... 6mA
- PROPAGATION DELAY: 40nsec @ 5V

TRUTH TABLE

<table>
<thead>
<tr>
<th>CONTROL INPUTS</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>E A E B</td>
<td></td>
</tr>
<tr>
<td>L L I 0 0</td>
<td>A B</td>
</tr>
<tr>
<td>L H I 0 0</td>
<td>A B</td>
</tr>
<tr>
<td>H L D O I</td>
<td>A B</td>
</tr>
<tr>
<td>H H ISOLATED</td>
<td>A B</td>
</tr>
</tbody>
</table>

I = Input, O = Output, D = Disconnected

HD-6434 CMOS OCTAL RESETTABLE LATCHED BUS DRIVER

FEATURES
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY .... 300pF
- SOURCE CURRENT .... 6mA
- SINK CURRENT ....... 9mA
- PROPAGATION DELAY: 45nsec @ 5V

TRUTH TABLE

<table>
<thead>
<tr>
<th>CONTROL INPUTS</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1 R2 R3 E1 E2 L1 L2</td>
<td>A Y</td>
</tr>
<tr>
<td>X X H H X X H I-Z</td>
<td></td>
</tr>
<tr>
<td>X X X H X X X X I-Z</td>
<td></td>
</tr>
<tr>
<td>L X L X L X X X L</td>
<td></td>
</tr>
<tr>
<td>X L L L L L L L L</td>
<td></td>
</tr>
<tr>
<td>H H L L L L L L</td>
<td></td>
</tr>
<tr>
<td>H H L L L L L X *</td>
<td></td>
</tr>
<tr>
<td>H H L L L L L X</td>
<td></td>
</tr>
</tbody>
</table>

X = Don't Care
H-I-Z = High Impedance
L = Low
H = High
* Data is latched to the value of the last input
I = Transition from a Low to High level
HD-6435 CMOS HEX RESETTABLE LATCHED BUS DRIVER

**FEATURES**
- Single Power Supply
- High Noise Immunity
- Industrial and Military Grades
- Drive Capacity: 300pF
- Source Current: 6mA
- Sink Current: 9mA
- Propagation Delay: 45nsec @ 5V

**TRUTH TABLE**

<table>
<thead>
<tr>
<th>Control Inputs</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1 R2 E1 E2 L1 L2</td>
<td>A Y</td>
</tr>
<tr>
<td>X X H X X X</td>
<td>H-I-Z</td>
</tr>
<tr>
<td>X X X H X</td>
<td>X-H-I-Z</td>
</tr>
<tr>
<td>L X L X X X</td>
<td>X</td>
</tr>
<tr>
<td>L L L X X</td>
<td>X</td>
</tr>
<tr>
<td>H H L L L L</td>
<td>L</td>
</tr>
<tr>
<td>H H L L L H</td>
<td>X</td>
</tr>
<tr>
<td>H H L L L H</td>
<td>X</td>
</tr>
<tr>
<td>H H L L L X</td>
<td>X</td>
</tr>
</tbody>
</table>

X = Don't Care
H-I-Z = High Impedance
H = High
L = Low
* Data is latched to the value of the last input
** = Transition from Low to High

**FUNCTIONAL DIAGRAM**

HD-6436 CMOS OCTAL BUS BUFFER/DIVIDE

**FEATURES**
- Single Power Supply
- High Noise Immunity
- Industrial and Military Grades
- Drive Capacity: 300pF
- Source Current: 6mA
- Sink Current: 9mA
- Propagation Delay: 45nsec @ 5V

**TRUTH TABLE**

<table>
<thead>
<tr>
<th>Control Inputs</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1 E2 A</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>L L L</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>L L H</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>L H X</td>
<td>HI-Z</td>
<td></td>
</tr>
<tr>
<td>H L X</td>
<td>HI-Z</td>
<td></td>
</tr>
<tr>
<td>H H X</td>
<td>HI-Z</td>
<td></td>
</tr>
</tbody>
</table>

L = Low, H = High, X = Don't Care
HI-Z = High Impedance

**FUNCTIONAL DIAGRAM**

HD-6440 CMOS LATCHED 3 TO 8 LINE DECODER-DRIVER

**FEATURES**
- High Speed Decoding for Memory Arrays
- Single Power Supply
- High Noise Immunity
- Industrial and Military Grades
- Drive Capacity: 200pF
- Source Current: 2mA
- Sink Current: 2.4mA
- Propagation Delay: 65nsec @ 5V

**TRUTH TABLE**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Address</th>
<th>Outputs</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1 E2 A2 A1</td>
<td>Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7</td>
<td>LATCHED</td>
<td>DECODE</td>
</tr>
</tbody>
</table>

L = Low, H = High, X = Don't Care
Yn = Data is latched to the value of the last input

**FUNCTIONAL DIAGRAM**

HD-6495 CMOS HEX BUS DRIVER

**FEATURES**
- Single Power Supply
- High Noise Immunity
- Industrial and Military Grades
- Drive Capacity: 300pF
- Source Current: 4mA
- Sink Current: 6mA
- Propagation Delay: 35nsec @ 5V

**TRUTH TABLE**

<table>
<thead>
<tr>
<th>Control Inputs</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1 E2 A</td>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>L L L</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>L L H</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>L H X</td>
<td>HI-Z</td>
<td></td>
</tr>
<tr>
<td>H L X</td>
<td>HI-Z</td>
<td></td>
</tr>
<tr>
<td>H H X</td>
<td>HI-Z</td>
<td></td>
</tr>
</tbody>
</table>

X = Don't Care
HI-Z = High Impedance

**FUNCTIONAL DIAGRAM**
Features

- HD-4702 – PROVIDES 13 COMMONLY USED BIT RATES
- HD-6405 – PROVIDES 15 COMMONLY USED BIT RATES
- USES A 2.4576MHz CRYSTAL/INPUT FOR STANDARD FREQUENCY OUTPUT (16 TIMES BIT RATE)
- TTL COMPATIBLE – OUTPUT WILL SINK 1.6mA
- LOW POWER DISSIPATION HD-6405 4.0mW TYP. @ 2.4576MHz
  HD-4702 4.5mW TYP. @ 2.4576MHz
- CONFORMS TO EIA RS-442
- ONE HD-4702 OR HD-6405 CONTROLS UP TO EIGHT TRANSMISSION CHANNELS
- INITIALIZATION CIRCUIT FACILITATES DIAGNOSTIC FAULT ISOLATION
- ON-CHIP INPUT PULL-UP CIRCUIT – HD-4702 ONLY

Description

The HD-4702/6405 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as UART. It generates 13 (HD-4702) or 15 (HD-6405) commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal +16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702/6405 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the +8 prescaler outputs Q0, Q1, Q2 available externally. All signals have a 50% duty cycle except 1800 Baud and 2000 Baud which has less than 0.39% distortion and 3600 Baud which has less than 0.78% distortion.

The four rate select inputs (S0-S3) select which bit rate is at the output (Z). The table lists select code and output bit rate. Two of the 16 for the HD-4702 and one of the 16 for the HD-6405 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate “ZERO BAUD”.

The bit rate most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single, 5-position switch.

The HD-4702/6405 has an initialization circuit which generates a common master reset for all flip-flops. This signal is derived from a digital differentiator that senses the first high level on the CP input after the ECP input goes low. When ECP is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset.

For the HD-4702, all inputs except IX have on-chip pull-up circuits which provide TTL compatibility and eliminate the need to tie a permanently high input to VCC.

Truth Tables

### Table 1: Clock Modes and Initialization

<table>
<thead>
<tr>
<th>IX</th>
<th>ECP</th>
<th>CP</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>Clocked from IX</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>Continuous Reset</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
<td>Restart during 1st CP - High Time</td>
</tr>
</tbody>
</table>

Note: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

H = High Level
L = Low Level
X = Don’t care
M = 1st High Level Clock Pulse after ECP goes LOW

### Table 2: Truth Table for Rate Select Inputs

<table>
<thead>
<tr>
<th>S3 S2 S1 S0</th>
<th>Output (1)</th>
<th>Output (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L L L L</td>
<td>MUX INPUT  (I1)</td>
<td>MUX INPUT  (I2)</td>
</tr>
<tr>
<td>L L L H</td>
<td>50 BAUD</td>
<td>50 BAUD</td>
</tr>
<tr>
<td>L L H L</td>
<td>75 BAUD</td>
<td>75 BAUD</td>
</tr>
<tr>
<td>L H L L</td>
<td>134.5 BAUD</td>
<td>134.5 BAUD</td>
</tr>
<tr>
<td>L L H L</td>
<td>200 BAUD</td>
<td>200 BAUD</td>
</tr>
<tr>
<td>H L L L</td>
<td>600 BAUD</td>
<td>600 BAUD</td>
</tr>
<tr>
<td>L H L H</td>
<td>2400 BAUD</td>
<td>2400 BAUD</td>
</tr>
<tr>
<td>H L H H</td>
<td>8600 BAUD</td>
<td>8600 BAUD</td>
</tr>
<tr>
<td>L H L L</td>
<td>4800 BAUD</td>
<td>4800 BAUD</td>
</tr>
<tr>
<td>H L H L</td>
<td>1800 BAUD</td>
<td>1800 BAUD</td>
</tr>
<tr>
<td>H L H H</td>
<td>3000 BAUD</td>
<td>3000 BAUD</td>
</tr>
<tr>
<td>H L H L</td>
<td>150 BAUD</td>
<td>150 BAUD</td>
</tr>
<tr>
<td>H L H L</td>
<td>110 BAUD</td>
<td>110 BAUD</td>
</tr>
</tbody>
</table>

Note: 19200 BAUD by connecting Q2 to IM.
ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th></th>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+12.0V</td>
<td>GND -0.3 to VCC +0.3</td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>-65°C to +150°C</td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td>-55°C to +125°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td>+4V to +11V</td>
</tr>
<tr>
<td>Industrial</td>
<td>HD-4702A-9/6405A-9</td>
<td></td>
</tr>
<tr>
<td>Military</td>
<td>HD-4702A-2/6405A-2</td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

D.C.: VCC = 10V ± 10%; TA = Industrial or Military.
A.C.: VCC = 10V; TA = 25°C.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>70% VCC</td>
<td>70% VCC</td>
<td></td>
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</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>20% VCC</td>
<td>20% VCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>VCC -0.1</td>
<td>VCC -0.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>GND +0.1</td>
<td>GND +0.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIH</td>
<td>Input High Current</td>
<td>-1</td>
<td>+1</td>
<td>+1 μA</td>
<td>VI = VCC, All other pins = 0V</td>
</tr>
<tr>
<td>III</td>
<td>INPUT (all other LOW inputs)</td>
<td>-110</td>
<td>-170</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIIX</td>
<td>OUTPUT (all other inputs)</td>
<td>+1</td>
<td>-1</td>
<td>+1 μA</td>
<td>VI = 0, All other pins = VCC</td>
</tr>
<tr>
<td>IOH</td>
<td>HIGH CURRENT (all inputs)</td>
<td>0.2</td>
<td>0.2</td>
<td>mA</td>
<td>VOUT = 9.5, per Logic Function or Truth Table</td>
</tr>
<tr>
<td>IOIN</td>
<td>LOW CURRENT (all inputs)</td>
<td>0.6</td>
<td>0.6</td>
<td>mA</td>
<td>VOUT = 9.5</td>
</tr>
<tr>
<td>IOL</td>
<td>OUTPUT (all other outputs)</td>
<td>0.2</td>
<td>0.2</td>
<td>mA</td>
<td>VOUT = 0.5V</td>
</tr>
<tr>
<td>SUPPLY</td>
<td>HD-4702A CURRENT (STATE)</td>
<td>1000</td>
<td>3000</td>
<td>μA</td>
<td>ECP = VCC, CP = 0, All other inputs = GND</td>
</tr>
<tr>
<td>CPU</td>
<td>HD-4702A CURRENT (STATE)</td>
<td>500</td>
<td>1000</td>
<td>μA</td>
<td>ECP = VCC, CP = 0, All other inputs = VCC</td>
</tr>
<tr>
<td>CPU</td>
<td>HD-4702A CURRENT (STATE)</td>
<td>500</td>
<td>500</td>
<td>μA</td>
<td>ECP = VCC, CP = 0, All other inputs = VCC or GND</td>
</tr>
</tbody>
</table>

D.C.

1. **Input Current** and *Quiescent Power Supply Current* are relatively higher for this device because of active pull-up circuits on all inputs except Ix. This is done for TTL compatibility.
2. Propagation Delays (IPLH and IPHL) and Output Transition Times (IIHL and ITTLH) will change with Output Load Capacitance (CL). Set-Up Times (ts), Hold Times (th), and Minimum Pulse Widths (tw) do not vary with load capacitance.
3. The first High Level Clock Pulse after ECP goes Low and must be at least 200ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the Clock Inputs (CP, Ix) be less than 4 μs.
5. For multichannel operation, Propagation Delay (CO to Qn) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 190ns.

A.C.
### Specifications HD-4702/6405

**Absolute Maximum Ratings**

- **Supply Voltage**: +8.0V
- **Input or Output Voltage Applied**: GND -0.3V to VCC +0.3V
- **Storage Temperature Range**: -65°C to +150°C
- **Operating Temperature Range**:
  - Industrial: HD-4702-9/6405-9
  - -40°C to +85°C
  - -55°C to +125°C
- **Operating Voltage Range**: +4 to +7V

**Electrical Characteristics**

D.C.: VCC = 5V ± 10%; TA = Industrial or Military.
A.C.: VCC = 5V; TA = 25°C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>HD-4702-2/6405-2</th>
<th>HD-4702-9/6405-9</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>VCC -1.5</td>
<td>VCC -1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>1.5</td>
<td>1.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOH1</td>
<td>Output High Voltage</td>
<td>VCC -0.5</td>
<td>VCC -0.5</td>
<td>V</td>
<td>I O H ≤ 1μA</td>
</tr>
<tr>
<td>VOLL</td>
<td>Output Low Voltage</td>
<td>0.05</td>
<td>0.05</td>
<td>V</td>
<td>I O L ≤ 1μA</td>
</tr>
<tr>
<td>tIH</td>
<td>Input High Current</td>
<td>-</td>
<td>+1</td>
<td>+1</td>
<td>μA</td>
</tr>
<tr>
<td>tIL</td>
<td>Input HD-4702 (all other LOW inputs)</td>
<td>-30</td>
<td>-30</td>
<td>-30</td>
<td>-50</td>
</tr>
<tr>
<td>tILX</td>
<td>Output HIGH (all other outputs)</td>
<td>-0.1</td>
<td>-0.1</td>
<td>-0.1</td>
<td>μA</td>
</tr>
<tr>
<td>tIOL</td>
<td>Output LOW (all other outputs)</td>
<td>0.1</td>
<td>0.1</td>
<td>mA</td>
<td>VOUT = VCC -5</td>
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<tr>
<td>ICC</td>
<td>Supply</td>
<td>HD-4702</td>
<td>500</td>
<td>1500</td>
<td>μA</td>
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<td></td>
<td>Current</td>
<td>HD-6405-2</td>
<td>150</td>
<td>150</td>
<td>μA</td>
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<tr>
<td></td>
<td>IDD</td>
<td>HD-6405-9</td>
<td>150</td>
<td>150</td>
<td>μA</td>
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<tr>
<td>tPLH</td>
<td>Propagation Delay, IX to CD</td>
<td>300</td>
<td>300</td>
<td>ns</td>
<td>CL ≤ 7pF on OX</td>
</tr>
<tr>
<td>tPPLH</td>
<td>Propagation Delay, CP to CD</td>
<td>250</td>
<td>250</td>
<td>ns</td>
<td>CL = 15pF Input Transition Times ≤ 20ns</td>
</tr>
<tr>
<td>tPHL</td>
<td>Propagation Delay, CO to Qn</td>
<td>215</td>
<td>215</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPPLH</td>
<td>Propagation Delay, CO to Z</td>
<td>195</td>
<td>195</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPLH</td>
<td>Propagation Delay, CP to CO</td>
<td>75</td>
<td>75</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPPLH</td>
<td>Propagation Delay, CO to Qn</td>
<td>65</td>
<td>65</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tTLL</td>
<td>Output Transition Time (except Ox)</td>
<td>80</td>
<td>80</td>
<td>ns</td>
<td>CL ≤ 7pF on OX</td>
</tr>
<tr>
<td>tTPLL</td>
<td>Propagation Delay, IX to CO</td>
<td>40</td>
<td>40</td>
<td>ns</td>
<td>CL = 50pF Input Transition Times ≤ 20ns</td>
</tr>
<tr>
<td>tPLL</td>
<td>Propagation Delay, CP to CO</td>
<td>350</td>
<td>350</td>
<td>ns</td>
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<tr>
<td>tPPLL</td>
<td>Propagation Delay, CO to Qn</td>
<td>275</td>
<td>275</td>
<td>ns</td>
<td></td>
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<tr>
<td>tPLL</td>
<td>Propagation Delay, CO to Z</td>
<td>220</td>
<td>220</td>
<td>ns</td>
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<tr>
<td>tTLL</td>
<td>Output Transition Time (except Ox)</td>
<td>85</td>
<td>85</td>
<td>ns</td>
<td>CL ≤ 7pF on OX</td>
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<tr>
<td>tTPLL</td>
<td>Propagation Delay, IX to CO</td>
<td>75</td>
<td>75</td>
<td>ns</td>
<td>CL = 15pF Input Transition Times ≤ 20ns</td>
</tr>
<tr>
<td>tPLL</td>
<td>Propagation Delay, CP to CO</td>
<td>350</td>
<td>350</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPPLL</td>
<td>Propagation Delay, CO to Qn</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPLL</td>
<td>Propagation Delay, CO to Z</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
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<tr>
<td>tTLL</td>
<td>Output Transition Time (except Ox)</td>
<td>85</td>
<td>85</td>
<td>ns</td>
<td>CL ≤ 7pF on OX</td>
</tr>
<tr>
<td>tTPLL</td>
<td>Propagation Delay, IX to CO</td>
<td>75</td>
<td>75</td>
<td>ns</td>
<td>CL = 15pF Input Transition Times ≤ 20ns</td>
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<tr>
<td>tPLL</td>
<td>Propagation Delay, CP to CO</td>
<td>350</td>
<td>350</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPPLL</td>
<td>Propagation Delay, CO to Qn</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPLL</td>
<td>Propagation Delay, CO to Z</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tTLL</td>
<td>Output Transition Time (except Ox)</td>
<td>160</td>
<td>160</td>
<td>ns</td>
<td>CL ≤ 7pF on OX</td>
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<tr>
<td>tTPLL</td>
<td>Propagation Delay, IX to CO</td>
<td>75</td>
<td>75</td>
<td>ns</td>
<td>CL = 50pF Input Transition Times ≤ 20ns</td>
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<td>0</td>
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<tr>
<td>tTLL</td>
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<td>160</td>
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<td>ns</td>
<td>CL ≤ 7pF on OX</td>
</tr>
<tr>
<td>tTPLL</td>
<td>Propagation Delay, IX to CO</td>
<td>75</td>
<td>75</td>
<td>ns</td>
<td>CL = 15pF Input Transition Times ≤ 20ns</td>
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<tr>
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<td>ns</td>
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<tr>
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<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
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<tr>
<td>tPLL</td>
<td>Propagation Delay, CO to Z</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tTLL</td>
<td>Output Transition Time (except Ox)</td>
<td>160</td>
<td>160</td>
<td>ns</td>
<td>CL ≤ 7pF on OX</td>
</tr>
<tr>
<td>tTPLL</td>
<td>Propagation Delay, IX to CO</td>
<td>75</td>
<td>75</td>
<td>ns</td>
<td>CL = 50pF Input Transition Times ≤ 20ns</td>
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<td>ns</td>
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<td>0</td>
<td>ns</td>
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<tr>
<td>tTLL</td>
<td>Output Transition Time (except Ox)</td>
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<td>160</td>
<td>ns</td>
<td>CL ≤ 7pF on OX</td>
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<td>75</td>
<td>75</td>
<td>ns</td>
<td>CL = 15pF Input Transition Times ≤ 20ns</td>
</tr>
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<td>350</td>
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<tr>
<td>tPPLL</td>
<td>Propagation Delay, CO to Qn</td>
<td>0</td>
<td>0</td>
<td>ns</td>
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<tr>
<td>tPLL</td>
<td>Propagation Delay, CO to Z</td>
<td>0</td>
<td>0</td>
<td>ns</td>
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</tr>
<tr>
<td>tTLL</td>
<td>Output Transition Time (except Ox)</td>
<td>160</td>
<td>160</td>
<td>ns</td>
<td>CL ≤ 7pF on OX</td>
</tr>
<tr>
<td>tTPLL</td>
<td>Propagation Delay, IX to CO</td>
<td>75</td>
<td>75</td>
<td>ns</td>
<td>CL = 50pF Input Transition Times ≤ 20ns</td>
</tr>
<tr>
<td>tPLL</td>
<td>Propagation Delay, CP to CO</td>
<td>350</td>
<td>350</td>
<td>ns</td>
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<tr>
<td>tPPLL</td>
<td>Propagation Delay, CO to Qn</td>
<td>0</td>
<td>0</td>
<td>ns</td>
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</tr>
<tr>
<td>tPLL</td>
<td>Propagation Delay, CO to Z</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tTLL</td>
<td>Output Transition Time (except Ox)</td>
<td>160</td>
<td>160</td>
<td>ns</td>
<td>CL ≤ 7pF on OX</td>
</tr>
</tbody>
</table>

**Notes:**

1. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except IX. This is done for TTL compatibility.
2. Propagation Delays (tPLH and tPPLH) and Output Transition Times (tTLL and tTPLL) will change with Output Load Capacitance (CL), Set-Up Times (tSL), Hold Times (tHL), and Minimum Pulse Widths (tWP) do not vary with load capacitance.
3. The first High Level Clock Pulse after ECP goes Low and must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the Clock Inputs (CP, 1X) be less than 15μs.
5. For multichannel operation, Propagation Delay (CO to Qn) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.
Switching Waveforms

NOTE: Set-Up and Hold Times are shown as positive values but may be specified as negative values.

Block Diagram

HD-4702 ONLY

VDD = PIN 16
VSS = PIN 8
□ = PIN NUMBER
Applications

SINGLE CHANNEL BIT RATE GENERATOR

Figure 1 shows the simplest application of the HD-4702/6405. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The Bit Rate Output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 or 3600 Baud. For many low cost terminals, these five bit rates are adequate.

SIMULTANEOUS GENERATION OF SEVERAL BIT RATES

Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one HD-4702/6405 and one 93L34 Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q0 to Q2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter Outputs back to the Select Inputs of the multiplexer causes the HD-4702/6405 to interrogate sequentially the state of eight different frequency signals. The 93L34 8 Bit Addressable Latch, addressed by the same Scan Counter Outputs, re-converts the multiplexed single Output (Z) of the HD-4702/6405 into eight parallel output frequency signals. In the simple scheme of Figure 2, input S3 is left open (HIGH) and the following bit rates are generated:

- Q0: 110 Baud
- Q1: 9600 Baud
- Q2: 4800 Baud
- Q3: 1800 Baud
- Q4: 1200 Baud
- Q5: 2400 Baud
- Q6: 300 Baud
- Q7: 150 Baud

Other bit rate combinations can be generated by changing the Scan Counter to Selector interconnection or by inserting logic gates into this path.

19200 BAUD OPERATION

Though a 19200 Baud signal is not internally routed to the multiplexer, the HD-4702/6405 can be used to generate this bit rate by connecting the Q2 output to the IM input and applying select code. An additional 2-input NOR gate can be used to retain the “Zero Baud” feature on select code 1 for the HD-4702 (See Figure 3).

![Figure 1](image1.png)

Switch selectable bit rate generator configuration providing five bit rates.

![Figure 2](image2.png)

Bit rate generator configuration with eight simultaneous frequencies

![Figure 3](image3.png)

19200 Baud Operation

### TABLE 3

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>TYPICAL CRYSTAL SPEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>2.4576 MHz “AT” Cut</td>
</tr>
<tr>
<td>Series Resistance</td>
<td>50</td>
</tr>
<tr>
<td>Unwanted Modes</td>
<td>-6 dB (Min)</td>
</tr>
<tr>
<td>Type of Operation</td>
<td>Parallel</td>
</tr>
<tr>
<td>Load Capacitance</td>
<td>32pF &lt;0.5</td>
</tr>
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</table>

NOTE 1: Need to add pull-up resistor on all inputs for the HD-6405.
Features

- OPERATION FROM D.C. TO 4.0MHz @10.0 VOLTS
- LOW POWER-TYP. 10mW @ 2.0MHz AND 5.0 VOLTS
- 4 TO 11 VOLT OPERATION
- PROGRAMMABLE WORD LENGTH, STOP BITS AND PARITY
- AUTOMATIC DATA FORMATTING AND STATUS GENERATION
- COMPATIBLE WITH INDUSTRY STANDARD UART'S
- SINGLE POWER SUPPLY

Description

The HD-6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits operation clock frequencies up to 4.0MHz (250K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Control Definition

<table>
<thead>
<tr>
<th>CONTROL WORD</th>
<th>CHARACTER FORMAT</th>
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</thead>
<tbody>
<tr>
<td>C C</td>
<td>START DATA PARITY STOP</td>
</tr>
<tr>
<td>L L P E S</td>
<td>BIT BITS BIT BITS</td>
</tr>
<tr>
<td>S S I P B</td>
<td>0 0 0 0 0 1 5 ODD 1</td>
</tr>
<tr>
<td></td>
<td>0 0 0 0 1 5 ODD 1.5</td>
</tr>
<tr>
<td></td>
<td>0 0 0 1 0 1 5 EVEN 1</td>
</tr>
<tr>
<td></td>
<td>0 0 0 1 0 1 5 EVEN 1.5</td>
</tr>
<tr>
<td></td>
<td>0 0 1 X 0 1 5 NONE 1</td>
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<td></td>
<td>0 0 1 X 1 5 NONE 1.5</td>
</tr>
<tr>
<td></td>
<td>0 1 0 0 0 1 6 ODD 1</td>
</tr>
<tr>
<td></td>
<td>0 1 0 0 1 6 ODD 2</td>
</tr>
<tr>
<td></td>
<td>0 1 0 1 0 1 6 EVEN 1</td>
</tr>
<tr>
<td></td>
<td>0 1 0 1 1 6 EVEN 2</td>
</tr>
<tr>
<td></td>
<td>0 1 1 X 0 1 6 NONE 1</td>
</tr>
<tr>
<td></td>
<td>0 1 1 X 1 6 NONE 2</td>
</tr>
<tr>
<td></td>
<td>1 0 0 0 0 1 7 ODD 1</td>
</tr>
<tr>
<td></td>
<td>1 0 0 0 1 7 ODD 2</td>
</tr>
<tr>
<td></td>
<td>1 0 1 0 0 1 7 EVEN 1</td>
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<tr>
<td></td>
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<tr>
<td></td>
<td>1 1 0 0 0 1 8 ODD 1</td>
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<td>1 1 1 X 0 1 8 NONE 1</td>
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<td></td>
<td>1 1 1 X 1 8 NONE 2</td>
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</table>

* These outputs are three state
Specifications HD-6402A

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Specification</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
<th>Conditions</th>
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<tbody>
<tr>
<td>VCC</td>
<td>10.0V ± 0.5V.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>±12.0V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V to VCC +0.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
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<td></td>
<td></td>
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</tr>
<tr>
<td>Industrial HD-6402A-9</td>
<td>-55°C to +125°C</td>
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</tr>
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</table>

ELECTRICAL CHARACTERISTICS

VCC = 10.0V ± 0.5V. TA = Industrial or Military

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<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MINIMUM</th>
<th>TYPICAL</th>
<th>MAXIMUM</th>
<th>UNITS</th>
<th>CONDITIONS</th>
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</thead>
<tbody>
<tr>
<td>D.C.</td>
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<td></td>
<td></td>
<td></td>
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<tr>
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<td>Logical ’1’ Input Voltage</td>
<td>70% VCC</td>
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<td>20% VCC</td>
<td>V</td>
<td>0V ≤ VIN ≤ VCC</td>
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<tr>
<td>VIL</td>
<td>Logical ’0’ Input Voltage</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td></td>
<td>1.0</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Logical ’1’ Output Voltage*</td>
<td>VCC -0.01</td>
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<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Logical ’0’ Output Voltage*</td>
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<td></td>
<td>GND +0.01</td>
<td>V</td>
<td>IOUT = 0</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td></td>
<td>1.0</td>
<td>μA</td>
<td>VCC ≤ 10.5V</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>5.0</td>
<td></td>
<td>500</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>Input Capacitance*</td>
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<td></td>
<td>8.0</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance*</td>
<td>6.0</td>
<td></td>
<td>10.0</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

*Guaranteed but not 100% tested.

A.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>CONDITIONS</th>
</tr>
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<td>6.0</td>
<td>D.C.</td>
<td>4.0</td>
<td>MHz</td>
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<td></td>
<td></td>
</tr>
<tr>
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<td>75</td>
<td></td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tMP</td>
<td>Pulse Width MR</td>
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<td></td>
<td>400</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tSET</td>
<td>Input Data Setup Time</td>
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<td></td>
<td>40</td>
<td>ns</td>
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<td>tHOLD</td>
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<td>ns</td>
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<td>70</td>
<td>ns</td>
<td></td>
<td></td>
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</table>

NOTE (1) All devices guaranteed at worst case limits. Room temperature, 10V data provided for information—not guaranteed.

Switching Waveforms

FIGURE 1
Data Input Cycle

FIGURE 2
Control Register Load Cycle

FIGURE 3
Status Flag Output Enable Time or Data Output Enable Time
Specifications HD-6402

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage</td>
<td>+0.3V</td>
<td></td>
<td>-0.3V</td>
<td>GND</td>
<td></td>
</tr>
<tr>
<td>Applied</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
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<td></td>
<td>+150°C</td>
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<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
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<td></td>
<td>+85°C</td>
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<td></td>
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<tr>
<td>Military HD-6402-2</td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%, TA = Industrial or Military

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MINIMUM</th>
<th>TYPICAL</th>
<th>MAXIMUM</th>
<th>UNITS</th>
<th>CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Logical “0” Input Voltage</td>
<td>-1.0</td>
<td>1.0</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Logical “1” Output Voltage</td>
<td>2.4</td>
<td></td>
<td>0.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IOL</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td></td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>VCC</td>
<td>Supply Current</td>
<td>7.0</td>
<td>8.0</td>
<td>10.0</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>Input Capacitance*</td>
<td>0.45</td>
<td></td>
<td>2.0</td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance*</td>
<td></td>
<td></td>
<td>2.0</td>
<td>mΩ</td>
<td></td>
</tr>
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</table>

*Guaranteed but not 100% tested

D.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>CONDITIONS</th>
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<td>D.C.</td>
<td>2.0</td>
<td>MHz</td>
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<td>150</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tMR</td>
<td>Pulse Width MR</td>
<td>350</td>
<td>400</td>
<td></td>
<td>ns</td>
<td>See Switching Time</td>
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<tr>
<td>tSET</td>
<td>Input Data Setup Time</td>
<td>50</td>
<td>50</td>
<td></td>
<td>ns</td>
<td>Waveforms 1, 2, 3</td>
</tr>
<tr>
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<td>Input Data Hold Time</td>
<td>60</td>
<td>60</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tEN</td>
<td>Output Enable Time</td>
<td>125</td>
<td>160</td>
<td></td>
<td>ns</td>
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</tr>
</tbody>
</table>

A.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
<th>CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>fclock</td>
<td>Clock Frequency</td>
<td>D.C.</td>
<td>3.0</td>
<td>D.C.</td>
<td>2.0</td>
<td>MHz</td>
</tr>
<tr>
<td>tpsw</td>
<td>Pulse Widths CRL, DRR, TBRL</td>
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<td>150</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tMR</td>
<td>Pulse Width MR</td>
<td>350</td>
<td>400</td>
<td></td>
<td>ns</td>
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<td>Input Data Setup Time</td>
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<td>ns</td>
<td>Waveforms 1, 2, 3</td>
</tr>
<tr>
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<tr>
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<td>Output Enable Time</td>
<td>125</td>
<td>160</td>
<td></td>
<td>ns</td>
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</tr>
</tbody>
</table>

NOTE 1 All devices guaranteed at worst case limits. Room temperature, 5V data provided for information—not guaranteed.

Transmitter Operation

The transmitter section accepts parallel data, formats it and transmits it in serial form on the TROutput terminal. A Data is loaded into the transmitter buffer register from the inputs TR1 through TR8 by a logic low on the TBRLoad input. Valid data must be present at least tSET prior to and tHOLD following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1. B The rising edge of TBRL clears TBREntry. 0 to 1 clock cycles later, data is transferred to the transmitter register; TBREntry is cleared; TBREntry is set high; and serial data transmission is started. Output data is clocked by TRClock. The clock rate is 16 times the data rate. C A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. D Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.
Specifications HD-6402C-9

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+8.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inout or Output Voltage Applied</td>
<td>-3.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C</td>
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<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS  

VCC = 5.0V ± 5%, TA = Industrial

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
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<td>Logical “1” Input Voltage</td>
<td>VCC</td>
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<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logical “0” Input Voltage</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Input Leakage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Logical “1” Output Voltage</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Logical “0” Output Voltage</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
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<td></td>
<td></td>
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<tr>
<td>Cin</td>
<td>Input Capacitance*</td>
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<tr>
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<td>Output Capacitance*</td>
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<td>10.0</td>
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</table>

D.C.

*Guaranteed but not 100% tested.

A.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>fclock</td>
<td>Clock Frequency</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPW</td>
<td>Pulse Widths CRL, DRR, TBRL</td>
<td>200</td>
<td>225</td>
<td>1.0</td>
</tr>
<tr>
<td>tMR</td>
<td>Pulse Width MR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tSET</td>
<td>Input Data Setup Time</td>
<td>60</td>
<td>75</td>
<td>90</td>
</tr>
<tr>
<td>tHOLD</td>
<td>Input Data Hold Time</td>
<td>75</td>
<td>90</td>
<td>90</td>
</tr>
<tr>
<td>tEN</td>
<td>Output Enable Time</td>
<td>150</td>
<td>190</td>
<td></td>
</tr>
</tbody>
</table>

VCC = 5.0V  
TA = 25°C

VCC = 5.0V ± 5%  
TA = Industrial

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information—not guaranteed.

Receiver Operation

Data is received in serial form at the RInput. When no data is being received, RInput must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. A low level on DRReset clears the DReady line. A During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. C 1 clock cycle later DReady is reset to a logic high, and FError is evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error. A logic high on PError indicates a parity error.
Start Bit Detection

The receiver uses a 16X clock for timing. The start bit could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±¼ clock cycle, ±1/32 bit or 3.125% giving a receiver margin of 46.875%. The receiver begins searching for the next start bit at the center of the first stop bit.
Typical Serial Data Link

The bit rate generator is shown supplying the transmit and receive clocks for the UART.

Interfacing With The 6402
HD-6408
CMOS Asynchronous Serial Manchester Adapter (ASMA)

Features

- LOW BIT ERROR RATE
- ONE MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- SINGLE POWER SUPPLY
- 24 PIN PACKAGE

Description

The HD-6408 is a CMOS/LSI Manchester Encoder/Decoder for creating a very high speed asynchronous serial data bus. The Encoder converts serial NRZ data (typically from a shift register) to Manchester II encoded data adding a sync pulse and parity bit. The Decoder recognizes this sync pulse and identifies it as a Command Sync or a Data Sync. The data is then decoded and shifted out in the NRZ code (typically into a shift register). Finally, the parity bit is checked. If there were no Manchester or parity errors the Decoder responds with a valid word signal. This Decoder puts the Manchester code to full use to provide clock recovery and excellent noise immunity at these very high speeds.

The HD-6408 can be used in many commercial applications such as, security systems, environmental control systems, serial data links and many others. It utilizes a single 12X clock and achieves data rates of up to one million bits per second with a very minimum overhead of only 4 bits out of 20, leaving 16 bits for data.

Block Diagrams

ENCODER

DECODER
### Specifications HD-6408-9

#### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>7.0V</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND</td>
<td>-0.3V</td>
<td>VEE</td>
<td>V</td>
<td>0V ≤ V IN ≤ VCC</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C</td>
<td></td>
<td>+150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C</td>
<td></td>
<td>+85°C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### ELECTRICAL CHARACTERISTICS

\( V_{CC} = 5.0V ±5\% \)  \( TA = -40°C \) to +85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical “1” Input Voltage</td>
<td>70% VCC</td>
<td>20% VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logical “0” Input Voltage</td>
<td></td>
<td></td>
<td>2.4 V</td>
<td></td>
</tr>
<tr>
<td>VHC</td>
<td>Logical “1” Input Voltage (Clock)</td>
<td>VCC -0.5</td>
<td>GND +0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VILC</td>
<td>Logical “0” Input Voltage (Clock)</td>
<td></td>
<td></td>
<td>0.4 V</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>VOH</td>
<td>Logical “1” Output Voltage</td>
<td>-0.1</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Logical “0” Output Voltage</td>
<td></td>
<td></td>
<td>1.8mA</td>
<td></td>
</tr>
<tr>
<td>ICCSB</td>
<td>Supply Current Standby</td>
<td>0.5</td>
<td>2</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>ICCOP</td>
<td>Supply Current Operating*</td>
<td>8.0</td>
<td>10.0</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>Input Capacitance*</td>
<td>5.0</td>
<td>7.0</td>
<td>pF</td>
<td>CL = 50pF</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance*</td>
<td>8.0</td>
<td>10.0</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

*Guaranteed and sampled but not 100% tested.

#### ENCODER TIMING

\( V_{CC} = 5.0V ±5\% \)  \( TA = -40°C \) to +85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEC</td>
<td>Encoder Clock Frequency</td>
<td>12 MHz</td>
<td></td>
</tr>
<tr>
<td>FESC</td>
<td>Send Clock Frequency</td>
<td>2.0 MHz</td>
<td></td>
</tr>
<tr>
<td>TECR</td>
<td>Encoder Clock Rise Time</td>
<td>8 ns</td>
<td></td>
</tr>
<tr>
<td>TECF</td>
<td>Encoder Clock Fall Time</td>
<td>8 ns</td>
<td></td>
</tr>
<tr>
<td>FED</td>
<td>Data Rate</td>
<td>1.0 MHz</td>
<td></td>
</tr>
<tr>
<td>TMR</td>
<td>Master Reset Pulse Width</td>
<td>150 ns</td>
<td></td>
</tr>
<tr>
<td>TE1</td>
<td>Shift Clock Delay</td>
<td>125 ns</td>
<td></td>
</tr>
<tr>
<td>TE2</td>
<td>Serial Data Setup</td>
<td>75 ns</td>
<td></td>
</tr>
<tr>
<td>TE3</td>
<td>Serial Data Hold</td>
<td>75 ns</td>
<td></td>
</tr>
<tr>
<td>TE4</td>
<td>Enable Setup</td>
<td>90 ns</td>
<td></td>
</tr>
<tr>
<td>TE5</td>
<td>Enable Pulse Width</td>
<td>80 ns</td>
<td></td>
</tr>
<tr>
<td>TE6</td>
<td>Sync Setup</td>
<td>55 ns</td>
<td></td>
</tr>
<tr>
<td>TE7</td>
<td>Sync Pulse Width</td>
<td>150 ns</td>
<td></td>
</tr>
<tr>
<td>TE8</td>
<td>Send Data Delay</td>
<td>50 ns</td>
<td></td>
</tr>
<tr>
<td>TE9</td>
<td>Bipolar Output Delay</td>
<td>130 ns</td>
<td></td>
</tr>
</tbody>
</table>

#### DECODER TIMING

\( V_{CC} = 5.0V ±5\% \)  \( TA = -40°C \) to +85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDC</td>
<td>Decoder Clock Frequency</td>
<td>12 MHz</td>
<td></td>
</tr>
<tr>
<td>TDCR</td>
<td>Decoder Clock Rise Time</td>
<td>8 ns</td>
<td></td>
</tr>
<tr>
<td>TDCF</td>
<td>Decoder Clock Fall Time</td>
<td>8 ns</td>
<td></td>
</tr>
<tr>
<td>FDD</td>
<td>Data Rate</td>
<td>1.0 MHz</td>
<td></td>
</tr>
<tr>
<td>TDR</td>
<td>Decoder Reset Pulse Width</td>
<td>150 ns</td>
<td></td>
</tr>
<tr>
<td>TDRS</td>
<td>Decoder Reset Setup Time</td>
<td>75 ns</td>
<td></td>
</tr>
<tr>
<td>TMR</td>
<td>Master Reset Pulse Width</td>
<td>150 ns</td>
<td></td>
</tr>
<tr>
<td>TD1</td>
<td>Bipolar Data Pulse Width</td>
<td>TDC +10</td>
<td></td>
</tr>
<tr>
<td>TD2</td>
<td>Sync Transition Span</td>
<td>18 TDC</td>
<td></td>
</tr>
<tr>
<td>TD3</td>
<td>One Zero Overlap</td>
<td>TDC -10</td>
<td></td>
</tr>
<tr>
<td>TD4</td>
<td>Short Data Transition Span</td>
<td>6 TDC</td>
<td></td>
</tr>
<tr>
<td>TD5</td>
<td>Long Data Transition Span</td>
<td>12 TDC</td>
<td></td>
</tr>
<tr>
<td>TD6</td>
<td>Sync Delay (ON)</td>
<td>40 ns</td>
<td></td>
</tr>
<tr>
<td>TD7</td>
<td>Take Data Delay (ON)</td>
<td>50 ns</td>
<td></td>
</tr>
<tr>
<td>TD8</td>
<td>Serial Data Out Delay</td>
<td>70 ns</td>
<td></td>
</tr>
<tr>
<td>TD9</td>
<td>Sync Delay (OFF)</td>
<td>90 ns</td>
<td></td>
</tr>
<tr>
<td>TD10</td>
<td>Take Data Delay (OFF)</td>
<td>90 ns</td>
<td></td>
</tr>
<tr>
<td>TD11</td>
<td>Valid Word Delay</td>
<td>90 ns</td>
<td></td>
</tr>
</tbody>
</table>

These parameters are guaranteed but not 100% tested.

\( TDC = \frac{15 \text{ TDC}}{15} = \frac{15 \text{ [Decoder Clock Period]}}{15} + 10ns \)

\( \text{FDC} = \frac{1}{15} \)
Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SClock input. An auxiliary divide by six counter is provided on-chip which can be utilized to produce the SClock by dividing the DClock.

The Encoder's cycle begins when EE is high during a falling edge of ESC. This cycle lasts for one word length or twenty ESC periods. At the next low-to-high transition of the ESC, a high at SS input actuates a Command sync or a low will produce a Data sync for that word. When the Encoder is ready to accept data, the SD output will go high and remain high for sixteen ESC periods.

During these sixteen periods the data should be clocked into the SD input with every high-to-low transition of the ESC. After the sync and Manchester II encoded data are transmitted through the BOO and BZO outputs, the Encoder adds an additional bit which is the (odd) parity for that word. At any time a low on SI will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MR. Any time after or during this pulse, a low-to-high transition on SC clears the internal counters and initializes the Encoder for a new word.

Decoder Operation

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DClock input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BOI and BZI inputs will accept data from a differential output comparator. The UDI input can only accept noninverted Manchester II coded data (e.g. from BZO of an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized, the type of sync is indicated by the CDS output. If the sync character was a command, this output will go high and remain high for sixteen DSC periods, otherwise it will remain low. The TD output will go high and remain high while the Decoder is transmitting the decoded data through SDO.

The decoded data available at SDO is in a NRZ format. The DSC is provided so that the decoded bits can get shifted into an external register on every low-to-high transition for this clock.

After all sixteen decoded bits have been transmitted, the data is checked for odd parity. A high on VW output indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

At any time in the above sequence a high input on DR during a low-to-high transition of DSC will abort transmission and initialize the Decoder to start looking for a new sync character.
## Pin Assignment and Functions

<table>
<thead>
<tr>
<th>PIN</th>
<th>SYMBOL</th>
<th>SECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VW</td>
<td>Decoder</td>
<td>Output high indicates receipt of a VALID WORD.</td>
</tr>
<tr>
<td>2</td>
<td>ESC</td>
<td>Encoder</td>
<td>ENCODER SHIFT CLOCK is an output for shifting data into the Encoder. This clock shifts data on a low-to-high transition.</td>
</tr>
<tr>
<td>3</td>
<td>TD</td>
<td>Decoder</td>
<td>TAKE DATA output is high during receipt of data after identification of a sync pulse.</td>
</tr>
<tr>
<td>4</td>
<td>SDO</td>
<td>Decoder</td>
<td>SERIAL DATA OUT delivers received data in correct NRZ format.</td>
</tr>
<tr>
<td>5</td>
<td>DC</td>
<td>Decoder</td>
<td>DECODER CLOCK input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder.</td>
</tr>
<tr>
<td>6</td>
<td>BZI</td>
<td>Decoder</td>
<td>A high input should be applied to BIPOLAR ZERO IN when the bus is in its negative state. This pin must be held high when the Unipolar input is used.</td>
</tr>
<tr>
<td>7</td>
<td>BOI</td>
<td>Decoder</td>
<td>A high input should be applied to BIPOLAR ONE IN when the bus is in its positive state, this pin must be held low when the Unipolar input is used.</td>
</tr>
<tr>
<td>8</td>
<td>UDI</td>
<td>Decoder</td>
<td>With pin 6 high and pin 7 low, this pin enters UNIPOLAR DATA IN to the transition finder circuit. If not used this input must be held low.</td>
</tr>
<tr>
<td>9</td>
<td>DSC</td>
<td>Decoder</td>
<td>DECODER SHIFT CLOCK output delivers a frequency (DECODER CLOCK / 12), synchronized by the recovered serial data stream.</td>
</tr>
<tr>
<td>10</td>
<td>CDS</td>
<td>Decoder</td>
<td>COMMAND/DATA SYNC output high occurs during output of decoded data which was preceded by a Command synchronizing character. A low output indicates a Data synchronizing character.</td>
</tr>
<tr>
<td>11</td>
<td>DR</td>
<td>Decoder</td>
<td>A high input to DECODER RESET during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>Both</td>
<td>GROUND supply pin.</td>
</tr>
</tbody>
</table>

### Diagram

![Diagram of HD-6408](image)

<table>
<thead>
<tr>
<th>PIN</th>
<th>SYMBOL</th>
<th>SECTION</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>MR</td>
<td>Both</td>
<td>A high on MASTER RESET clears the 2:1 counters in both the encoder and decoder.</td>
</tr>
<tr>
<td>14</td>
<td>DBS</td>
<td>Encoder</td>
<td>DIVIDE BY SIX is an output from 6:1 divider which is driven by the ENCODER CLOCK.</td>
</tr>
<tr>
<td>15</td>
<td>BZO</td>
<td>Encoder</td>
<td>BIPOLAR ZERO OUT is an active low output designed to drive the zero or negative sense of a bipolar line driver.</td>
</tr>
<tr>
<td>16</td>
<td>OI</td>
<td>Encoder</td>
<td>A low on OUTPUT INHIBIT forces pin 15 and 17 high, their inactive states.</td>
</tr>
<tr>
<td>17</td>
<td>BOO</td>
<td>Encoder</td>
<td>BIPOLAR ONE OUT is an active low output designed to drive the one or positive sense of a bipolar line driver.</td>
</tr>
<tr>
<td>18</td>
<td>SDI</td>
<td>Encoder</td>
<td>SERIAL DATA IN accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.</td>
</tr>
<tr>
<td>19</td>
<td>EE</td>
<td>Encoder</td>
<td>A high on ENCODER ENABLE initiates the encode cycle. (Subject to the preceding cycle being completed.)</td>
</tr>
<tr>
<td>20</td>
<td>SS</td>
<td>Encoder</td>
<td>SYNC SELECT actuates a Command sync for an input high and Data sync for an input low.</td>
</tr>
<tr>
<td>21</td>
<td>SD</td>
<td>Encoder</td>
<td>SEND DATA is an active high output which enables the external source of serial data.</td>
</tr>
<tr>
<td>22</td>
<td>SCI</td>
<td>Encoder</td>
<td>SEND CLOCK IN is 2X the Encoder data rate.</td>
</tr>
<tr>
<td>23</td>
<td>EC</td>
<td>Encoder</td>
<td>ENCODER CLOCK is the input to the 6:1 divider.</td>
</tr>
<tr>
<td>24</td>
<td>VCC</td>
<td>Both</td>
<td>Positive supply pin.</td>
</tr>
</tbody>
</table>
**Features**

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY: 300pF
- SOURCE CURRENT: 4mA
- SINK CURRENT: 6mA
- PROPAGATION DELAY: 65nsec @ 5V

**Description**

The HD-6431 is a self-aligned silicon gate CMOS Latching Three-State Bus Driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A high on the strobe line L allows data to go through the latches and a transition to low latches the data. A high on the Three-State control \( \bar{E} \) forces the buffers to the high impedance mode without disturbing the latched data. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

**Truth Table**

<table>
<thead>
<tr>
<th>CONTROL INPUTS</th>
<th>DATA PORT STATUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \bar{E} )</td>
<td>A</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L ( \uparrow )</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

* Data is latched to the value of the last input  
X = Don’t Care  
HI-Z = High Impedance  
\( \uparrow \) = Transition from High to Low level

**Pinout**

<table>
<thead>
<tr>
<th>TOP VIEW</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
</tr>
<tr>
<td>1A</td>
</tr>
<tr>
<td>1Y</td>
</tr>
<tr>
<td>2A</td>
</tr>
<tr>
<td>2Y</td>
</tr>
<tr>
<td>3A</td>
</tr>
<tr>
<td>3Y</td>
</tr>
<tr>
<td>GND</td>
</tr>
</tbody>
</table>

**Functional Diagram**

[Diagram of the HD-6431 CMOS Hex Latching Bus Driver]
Specifications HD-6431A

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td></td>
<td>+12.0V</td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td></td>
<td>-0.3V to VCC +0.3V</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td>-65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td>-40°C to +85°C</td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6431A-9</td>
<td></td>
<td>-55°C to +125°C</td>
<td></td>
</tr>
<tr>
<td>Military HD-6431A-2</td>
<td></td>
<td>+4 to +11V</td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

\[ V_{CC} = 10V \pm 10\%; T_A = \text{Industrial or Military} \]

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% ( V_{CC} )</td>
<td>V</td>
<td></td>
<td>( 0V \leq V_{IN} \leq V_{CC} )</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>20% ( V_{CC} )</td>
<td>V</td>
<td></td>
<td>( E = \text{Low} )</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-10</td>
<td>10 ( \mu A )</td>
<td></td>
<td>( I_{OL} = -8.0mA, )</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>VCC -0.4</td>
<td>V</td>
<td></td>
<td>( E = \text{High} )</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>0.4</td>
<td>V</td>
<td></td>
<td>( 0V \leq V_{O} \leq V_{CC} )</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-10</td>
<td>10 ( \mu A )</td>
<td></td>
<td>( V_{IN} = V_{CC} ) or GND,</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>100</td>
<td>( \mu A )</td>
<td></td>
<td>( V_{CC} = 11V )</td>
</tr>
<tr>
<td>CIN</td>
<td>Input Capacitance*</td>
<td>5</td>
<td>pF</td>
<td></td>
<td>( V_{IN} = 0V, T_A = 25^\circ C; )</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance*</td>
<td>15</td>
<td>pF</td>
<td></td>
<td>( f = 1\text{MHz} )</td>
</tr>
</tbody>
</table>

* Guaranteed and sampled, but not 100% tested.

\[ C_L = 300pF \]

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>V_{CC} = 10.0V ( 25^\circ C )</th>
<th>V_{CC} = 10.0V ( \pm 10% )</th>
</tr>
</thead>
<tbody>
<tr>
<td>A.C.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( T_A = \text{Indust. or Mil.} )</td>
<td>( T_A = \text{Indust. or Mil.} )</td>
</tr>
<tr>
<td>tPD</td>
<td>Propagation Delay</td>
<td>35</td>
<td>45</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tEN</td>
<td>Enable Time</td>
<td>35</td>
<td>45</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tDIS</td>
<td>Disable Time</td>
<td>35</td>
<td>45</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tSET</td>
<td>Input Set Up Time</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tHOLD</td>
<td>Input Hold Time</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tPW</td>
<td>Pulse Width</td>
<td>15</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tR</td>
<td>Output Rise Time</td>
<td>30</td>
<td>40</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tF</td>
<td>Output Fall Time</td>
<td>20</td>
<td>30</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE**: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information—not guaranteed.
Specifications HD-6431

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+8.0V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V to VCC +0.3V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military HD-6431-2</td>
<td>-55°C to +125°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td>+4 to +7V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

\( V_{CC} = 5.0V \pm 10\% \); \( T_A = \) Industrial or Military

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH} )</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% ( V_{CC} )</td>
<td>( V )</td>
<td>( 0V \leq V_{IN} \leq V_{CC} )</td>
<td></td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>20% ( V_{CC} )</td>
<td>( V )</td>
<td>( 0V \leq V_{IN} \leq V_{CC} )</td>
<td>( I_{OH} = -4.0mA, ) ( E = ) Low</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>( \mu A )</td>
<td>( 0V \leq V_{IN} \leq V_{CC} )</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>( V_{CC} -0.4 )</td>
<td>( V )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>0.4</td>
<td>( V )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{O} )</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>( \mu A )</td>
<td>( 0V \leq V_{O} \leq V_{CC} )</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Supply Current</td>
<td>10</td>
<td>( \mu A )</td>
<td>( V_{IN} = V_{CC} ) or GND, ( V_{CC} = 5.5V )</td>
<td>( V_{IN} = 0V; T_A = 25^\circ C; ) ( f = 1MHz )</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance*</td>
<td>5</td>
<td>( pF )</td>
<td></td>
<td>( V_{IN} = 0V; T_A = 25^\circ C; ) ( f = 1MHz )</td>
</tr>
<tr>
<td>( C_{O} )</td>
<td>Output Capacitance*</td>
<td>15</td>
<td>( pF )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* Guaranteed and sampled, but not 100% tested.

\( C_L = 300pF \)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>( V_{CC} = 5.0V ) ( 25^\circ C )</th>
<th>( V_{CC} = 5.0V \pm 10% ) ( T_A = ) Indus. or Mil.</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PD} )</td>
<td>Propagation Delay</td>
<td>65 ns</td>
<td>75 ns</td>
</tr>
<tr>
<td>( t_{EN} )</td>
<td>Enable Time</td>
<td>80 ns</td>
<td>90 ns</td>
</tr>
<tr>
<td>( t_{DIS} )</td>
<td>Disable Time</td>
<td>80 ns</td>
<td>90 ns</td>
</tr>
<tr>
<td>( t_{SET} )</td>
<td>Input Setup Time</td>
<td>15 ns</td>
<td>15 ns</td>
</tr>
<tr>
<td>( t_{HOLD} )</td>
<td>Input Hold Time</td>
<td>15 ns</td>
<td>15 ns</td>
</tr>
<tr>
<td>( t_{PW} )</td>
<td>Pulse Width</td>
<td>25 ns</td>
<td>30 ns</td>
</tr>
<tr>
<td>( t_{R} )</td>
<td>Output Rise Time</td>
<td>80 ns</td>
<td>90 ns</td>
</tr>
<tr>
<td>( t_{F} )</td>
<td>Output Fall Time</td>
<td>70 ns</td>
<td>80 ns</td>
</tr>
</tbody>
</table>

NOTE: All devices guaranteed at worst case limits. Room temperature, \( 5V \) data provided for information—not guaranteed.
Switching Waveforms

All inputs have \( t_R, t_F \leq 20\text{ns} \).

OUTPUT TEST CIRCUIT FOR PROPAGATION DELAYS

OUTPUT TEST CIRCUIT FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by \( I_T = C \frac{dV}{dt} \). Assuming that all outputs may change state at the same time and that \( \frac{dV}{dt} \) is constant, \( I_T = \sum C_L \left( \frac{V_{CC} \times 80\%}{t_R \text{ or } t_F} \right) \) eg. \( t_R = 80\text{ns}, V_{CC} = 5.0\text{V}, \) each \( C_L = 300\text{pF}, I_T = (4) \left( 300 \times 10^{-12} \right) \frac{5.0 \times 0.8}{80 \times 10^{-9}} = 90\text{mA} \). This current spike may cause a large negative voltage spike on \( V_{CC} \), which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 \( \mu \text{F} \) ceramic disk decoupling capacitor be placed between \( V_{CC} \) and GND at each device to filter out this noise.

PROPAGATION DELAYS

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of \( \pm 10\% \), an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6431-2. The table of A.C. specs shows the \( t_{PD} \) at 4.5V and 125°C is 75nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10\% or 90\% point, is therefore 75 \times 0.84 or 63nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it’s degradation multiple to be 0.65. The adjusted rise time is, therefore, 90 \times 0.65 or 58nsec. To obtain the standard 50\% to 50\% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 92nsec. The rise time was used here because it is always the worst case.
**Features**

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY: 300pF
- SOURCE CURRENT: 4mA
- SINK CURRENT: 6mA
- PROPAGATION DELAY: 45nsec @ 5V

**Description**

The HD-6432 is a self-aligned silicon gate CMOS bi-directional bus driver. This circuit consists of 12 drivers organized as 6 bi-directional pairs. Four enable lines select drive direction or Three-State mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

**Truth Table**

<table>
<thead>
<tr>
<th>CONTROL INPUTS</th>
<th>DATA PORT STATUS</th>
</tr>
</thead>
<tbody>
<tr>
<td>EAB  EAB EBA EB</td>
<td>A      B</td>
</tr>
<tr>
<td>L X H L O I</td>
<td></td>
</tr>
<tr>
<td>X H H L O I</td>
<td></td>
</tr>
<tr>
<td>H L X H I O</td>
<td></td>
</tr>
<tr>
<td>L X L X I O</td>
<td></td>
</tr>
<tr>
<td>X H X H ISOLATED</td>
<td></td>
</tr>
<tr>
<td>L X X H ISOLATED</td>
<td></td>
</tr>
<tr>
<td>X H L X ISOLATED</td>
<td></td>
</tr>
<tr>
<td>H L H L NOT ALLOWED</td>
<td></td>
</tr>
</tbody>
</table>

I = Input, O = Output, X = Don't Care

**Functional Diagram**

[Diagram of the HD-6432 CMOS HEX BI-DIRECTIONAL BUS DRIVER]
# Specifications HD-6432A

## ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+12.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V</td>
<td>VCC +0.3V</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6432A-9</td>
<td>-40°C to +85°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military HD-6432A-2</td>
<td>-55°C to +125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td></td>
<td>+4 to +11V</td>
<td></td>
</tr>
</tbody>
</table>

## ELECTRICAL CHARACTERISTICS

V<sub>CC</sub> = 10V ± 10%; TA = Industrial or Military

### D.C.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>PARAMETER</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>20% V&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>V</td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; ≤ V&lt;sub&gt;IN&lt;/sub&gt; ≤ V&lt;sub&gt;CC&lt;/sub&gt;</td>
</tr>
<tr>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>-10</td>
<td>10</td>
<td>μA</td>
<td>I&lt;sub&gt;OH&lt;/sub&gt; = -8.0mA, I&lt;sub&gt;OL&lt;/sub&gt; = 12mA</td>
</tr>
<tr>
<td>I&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>Input Leakage</td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt; ≤ 0V ≤ V&lt;sub&gt;O&lt;/sub&gt; ≤ V&lt;sub&gt;CC&lt;/sub&gt;</td>
</tr>
<tr>
<td>V&lt;sub&gt;OH&lt;/sub&gt;</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td></td>
<td></td>
<td></td>
<td>E&lt;sub&gt;AB&lt;/sub&gt; = E&lt;sub&gt;BA&lt;/sub&gt; = Low</td>
</tr>
<tr>
<td>V&lt;sub&gt;OL&lt;/sub&gt;</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = V&lt;sub&gt;CC&lt;/sub&gt; or GND, V&lt;sub&gt;CC&lt;/sub&gt; = 11V</td>
</tr>
<tr>
<td>I&lt;sub&gt;O&lt;/sub&gt;</td>
<td>Output Leakage</td>
<td>-10</td>
<td>10</td>
<td>μA</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 0V; T&lt;sub&gt;A&lt;/sub&gt; = 25°C; f = 1MHz</td>
</tr>
<tr>
<td>I&lt;sub&gt;CC&lt;/sub&gt;</td>
<td>Supply Current</td>
<td>100</td>
<td></td>
<td>μA</td>
<td>V&lt;sub&gt;IN&lt;/sub&gt; = 0V; T&lt;sub&gt;A&lt;/sub&gt; = 25°C; f = 1MHz</td>
</tr>
<tr>
<td>C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input Capacitance*</td>
<td>5</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>C&lt;sub&gt;I/O&lt;/sub&gt;</td>
<td>I/O Capacitance*</td>
<td>20</td>
<td></td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

* Guaranteed and sampled, but not 100% tested.

### A.C.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>Max</th>
<th>Units</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>τ&lt;sub&gt;PD&lt;/sub&gt;</td>
<td>Propagation Delay</td>
<td>35</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>τ&lt;sub&gt;EN&lt;/sub&gt;</td>
<td>Enable Time</td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>τ&lt;sub&gt;DIS&lt;/sub&gt;</td>
<td>Disable Time</td>
<td>75</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>τ&lt;sub&gt;R&lt;/sub&gt;</td>
<td>Output Rise Time</td>
<td>40</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>τ&lt;sub&gt;F&lt;/sub&gt;</td>
<td>Output Fall Time</td>
<td>35</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

### Note

All devices guaranteed at worst case limits. Room temperature, 10V data provided for information—not guaranteed.

CL = 300pF

## Note

1. All devices guaranteed at worst case limits. Room temperature, 10V data provided for information—not guaranteed.
## Specifications HD-6432

### ABSOLUTE MAXIMUM RATINGS

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<th>Parameter</th>
<th>MIN</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+8.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>-0.3V to VCC</td>
<td>+0.3V</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6432-9</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Military HD-6432-2</td>
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<td></td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td>+4 to +7V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS

**VCC = 5.0V ± 10%; TA = Industrial or Military**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
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</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td></td>
<td>V</td>
<td>0V ≤ VIN ≤ VCC, I&lt;sub&gt;OH&lt;/sub&gt; = -4.0mA, VCC = 5.5V</td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>20% VCC</td>
<td>1.0</td>
<td>μA</td>
<td>0V ≤ VIN ≤ VCC, I&lt;sub&gt;OL&lt;/sub&gt; = 6.0mA</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td></td>
<td></td>
<td></td>
<td>E&lt;sub&gt;AB&lt;/sub&gt; = E&lt;sub&gt;B&lt;/sub&gt; = Low, VIN = VCC or GND, VCC = 5.5V, E&lt;sub&gt;OE&lt;/sub&gt; = V&lt;sub&gt;EE&lt;/sub&gt;</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>VCC -0.4</td>
<td></td>
<td>V</td>
<td>VIN = 0V; TA = 25°C; f = 1MHz</td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>0.4</td>
<td>1.0</td>
<td>μA</td>
<td>VIN = 0V; TA = 25°C; f = 1MHz</td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td></td>
<td></td>
<td>VIN = 0V; TA = 25°C; f = 1MHz</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>10</td>
<td>10</td>
<td>μA</td>
<td>VIN = 0V; TA = 25°C; f = 1MHz</td>
</tr>
<tr>
<td>C&lt;sub&gt;IN&lt;/sub&gt;</td>
<td>Input Capacitance*</td>
<td>5</td>
<td>5</td>
<td>pF</td>
<td>VIN = 0V; TA = 25°C; f = 1MHz</td>
</tr>
<tr>
<td>C&lt;sub&gt;I/O&lt;/sub&gt;</td>
<td>I/O Capacitance*</td>
<td>20</td>
<td>20</td>
<td>pF</td>
<td>VIN = 0V; TA = 25°C; f = 1MHz</td>
</tr>
</tbody>
</table>

* Guaranteed and sampled, but not 100% tested.

### D.C.

- **C<sub>L</sub> = 300pF**

### A.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>t&lt;sub&gt;PD&lt;/sub&gt;</td>
<td>Propagation Delay</td>
<td>45</td>
<td>55</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;EN&lt;/sub&gt;</td>
<td>Enable Time</td>
<td>65</td>
<td>75</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;DIS&lt;/sub&gt;</td>
<td>Disable Time</td>
<td>100</td>
<td>110</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;R&lt;/sub&gt;</td>
<td>Output Rise Time</td>
<td>100</td>
<td>110</td>
<td>ns</td>
</tr>
<tr>
<td>t&lt;sub&gt;F&lt;/sub&gt;</td>
<td>Output Fall Time</td>
<td>70</td>
<td>80</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTE**: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information—not guaranteed.
Switching Waveforms

All inputs have $t_R, t_F \leq 20\text{ns}$.

![Diagram of waveforms](image)

**OUTPUT TEST CIRCUIT FOR PROPAGATION DELAYS**

**OUTPUT TEST CIRCUIT FOR THREE-STATE DELAYS**

### DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C \frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = (\Sigma C_L) \left( \frac{V_{CC} \times 80\%}{t_R \text{ or } t_F} \right)$. Example: $t_R = 100\text{ns}$, $V_{CC} = 5.0\text{V}$ each $C_L = 300\text{pF}$, $I_T = (6) \left( \frac{300 \times 10^{-12} \times 5.0 \times 0.8}{100 \times 10^{-9}} \right) = 72\text{mA}$. This current spike may cause a large negative voltage spike on $V_{CC}$, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a $0.1\ \mu\text{F}$ ceramic disk decoupling capacitor be placed between $V_{CC}$ and GND at each device to filter out this noise.

### PROPAGATION DELAYS

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of $\pm 10\%$, an ambient temperature of as high as $125^\circ\text{C}$, and a calculated load capacitance of $150\text{pF}$. This application requires the HD-6432-2. The tables of A.C. specs shows the $t_{PD}$ at 4.5V and $125^\circ\text{C}$ is 55nsec. Use the graph in Figure 1 to get the degradation multiple for $150\text{pF}$. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore $55 \times 0.84$ or 46nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and $125^\circ\text{C}$ to obtain a worst case rise time of 110nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, $110 \times 0.65$ or 72nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 82nsec. The rise time was used here because it is always the worst case.
Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY ........................................... 300pF
- SOURCE CURRENT ........................................... 4mA
- SINK CURRENT ........................................... 6mA
- PROPAGATION DELAY ................................. 40nsec @ 5V

Description

The HD-6433 is a self-aligned silicon gate CMOS bus separator/driver. This circuit consists of 8 drivers organized as 4 pairs of bus separators which allow a unidirectional input bus and a unidirectional output bus to be interfaced with a bi-directional bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

<table>
<thead>
<tr>
<th>CONTROL</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EA</td>
<td>EB</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

I = Input, O = Output, D = Disconnected
Specifications HD-6433A

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+12.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND</td>
<td>-0.3V to VCC +0.3V</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6433A-9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military HD-6433A-2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td>+4 to +11V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

$V_{CC} = 10V \pm 10\%; \ T_A = \text{Industrial or Military}$

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Logical “1” Input Voltage</td>
<td>70% $V_{CC}$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logical “0” Input Voltage</td>
<td>20% $V_{CC}$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Leakage</td>
<td>-10</td>
<td>10</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Logical “1” Output Voltage</td>
<td>$V_{CC} - 0.4$</td>
<td>$V$</td>
<td>$I_{OH} = -8.0mA$</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Logical “0” Output Voltage</td>
<td>0.4</td>
<td>10</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{O}$</td>
<td>Output Leakage</td>
<td>-10</td>
<td>10</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>100</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance*</td>
<td>5</td>
<td></td>
<td>$pF$</td>
</tr>
<tr>
<td>$C_{I/O}$</td>
<td>I/O Capacitance*</td>
<td>20</td>
<td></td>
<td>$pF$</td>
</tr>
<tr>
<td>$C_{O}$</td>
<td>Output Capacitance*</td>
<td>15</td>
<td></td>
<td>$pF$</td>
</tr>
</tbody>
</table>

**D.C.**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>$V_{CC} = 10.0V \pm 10% \ T_A = \text{Indust. or Mil.}$</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PD}$</td>
<td>Propagation Delay</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{EN}$</td>
<td>Enable Time</td>
<td>45</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{DIS}$</td>
<td>Disable Time</td>
<td>45</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{R}$</td>
<td>Output Rise Time</td>
<td>65</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{F}$</td>
<td>Output Fall Time</td>
<td>55</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTE**
All devices guaranteed at worst case limits. Room temperature, 10V data provided for information—not guaranteed.
### Specifications HD-6433

#### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td></td>
<td>+8.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6433-9</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military HD-6433-2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V \pm 10\%; \ TA = \text{Industrial or Military}$

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% $V_{CC}$</td>
<td>$V$</td>
<td>$V$</td>
<td>$0V \leq V_{IN} \leq V_{CC}$</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>20% $V_{CC}$</td>
<td>$V$</td>
<td>$V$</td>
<td>$I_{OH} = -4.0mA$</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>$\mu A$</td>
<td>$I_{OL} = 6.0mA$</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>$V_{CC} - 0.4$</td>
<td>$V$</td>
<td>$I_{OH} = 4.0mA$</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>0.4</td>
<td>$V$</td>
<td>$I_{OL} = -6.0mA$</td>
<td></td>
</tr>
<tr>
<td>$I_{O}$</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>$\mu A$</td>
<td>$0V \leq V_{O} \leq V_{CC}$</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>Supply Current</td>
<td>10</td>
<td>$\mu A$</td>
<td>$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.5V$</td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance*</td>
<td>5</td>
<td>$pF$</td>
<td>$V_{IN} = 0V; TA = 25^0C; f = 1MHz$</td>
<td></td>
</tr>
<tr>
<td>$C_{I/O}$</td>
<td>I/O Capacitance*</td>
<td>20</td>
<td>$pF$</td>
<td>$V_{IN} = 0V; TA = 25^0C; f = 1MHz$</td>
<td></td>
</tr>
<tr>
<td>$C_{O}$</td>
<td>Output Capacitance*</td>
<td>15</td>
<td>$pF$</td>
<td>$V_{IN} = 0V; TA = 25^0C; f = 1MHz$</td>
<td></td>
</tr>
</tbody>
</table>

* Guaranteed and sampled, but not 100% tested.

$C_{L} = 300pF$

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>V_{CC} = 5.0V \text{ 25}^0C</th>
<th>V_{CC} = 5.0V \pm 10% \text{ TA = Indust. or Mil.}</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PD}$</td>
<td>Propagation Delay</td>
<td>40</td>
<td>50</td>
<td>ns</td>
<td>60</td>
<td>70</td>
</tr>
<tr>
<td>$t_{EN}$</td>
<td>Enable Time</td>
<td>60</td>
<td>70</td>
<td>ns</td>
<td>90</td>
<td>100</td>
</tr>
<tr>
<td>$t_{DIS}$</td>
<td>Disable Time</td>
<td>90</td>
<td>100</td>
<td>ns</td>
<td>85</td>
<td>95</td>
</tr>
<tr>
<td>$t_{R}$</td>
<td>Output Rise Time</td>
<td>85</td>
<td>80</td>
<td>ns</td>
<td>70</td>
<td>80</td>
</tr>
<tr>
<td>$t_{F}$</td>
<td>Output Fall Time</td>
<td>70</td>
<td>80</td>
<td>ns</td>
<td>85</td>
<td>95</td>
</tr>
</tbody>
</table>

**NOTE**: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information—not guaranteed.
Switching Waveforms

All inputs have $t_R, t_F \leq 20\text{ns}$.

OUTPUT TEST CIRCUIT FOR PROPAGATION DELAYS

OUTPUT TEST CIRCUIT FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C \frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left( \sum C_L \left( \frac{V_{CC} \times 80\%}{t_R \text{ or } t_F} \right) \right)$ eg. $t_R = 85\text{ns}$, $V_{CC} = 5.0\text{V}$, each $C_L = 300\text{pF}$, $I_T = (4) \left( 300 \times 10^{-12} \right) \frac{5.0 \times 0.8}{85 \times 10^{-9}} = 56.5\text{mA}$. This current spike may cause a large negative voltage spike on $V_{CC}$, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 $\mu\text{F}$ ceramic disk decoupling capacitor be placed between $V_{CC}$ and GND at each device to filter out this noise.

PROPAGATION DELAYS

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of \( \pm 10\% \), an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6433-2. The table of A.C. specs shows the $t_{PD}$ at 4.5V and 125°C is 50ns. The adjusted propagation delay, to the 10\% or 90\% point, is therefore $50 \times 0.84$ or 42ns. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95ns. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62ns. To obtain the standard 50\% to 50\% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 73ns. The rise time was used here because it is always the worst case.
**Features**

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY .................. 300pF
- SOURCE CURRENT .................. 6mA
- SINK CURRENT ..................... 9mA
- PROPAGATION DELAY ............ 45nsec @ 5V

**Description**

The HD-6434 is a self-aligned silicon gate CMOS latching Three State bus driver. This circuit consists of 8 non-inverting latching drivers with separate input and output. A low on both strobe lines (E) allows data to go through the latches and a transition to high latches the data. A high on either Three State control (E) forces the buffers to the high impedance mode without disturbing the latched data. A low on either reset line (R) forces each of the latches to a low level. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

**Truth Table**

<table>
<thead>
<tr>
<th>CONTROL INPUTS</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1, R2, E1, E2, C1, C2</td>
<td>A, Y</td>
</tr>
<tr>
<td>X, X, X, X, X, X</td>
<td>X, Hi-Z</td>
</tr>
<tr>
<td>L, X, L, L, X, X</td>
<td>L</td>
</tr>
<tr>
<td>X, L, L, L, X, X</td>
<td>L</td>
</tr>
<tr>
<td>H, H, L, L, L, L</td>
<td>H</td>
</tr>
</tbody>
</table>

X = Don't Care  Hi-Z = High Impedance  L = Low
H = High  * = Data is latched to the value of the last input
† = Transition from a Low to High level

**Functional Diagram**

[Diagram showing the circuit's functional layout]
Specifications HD-6434

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+8.0V</td>
<td>GND -0.3V to VCC +0.3V</td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6434-9</td>
<td></td>
<td>-40°C to +85°C</td>
<td></td>
</tr>
<tr>
<td>Military HD-6434-2</td>
<td></td>
<td>-55°C to +125°C</td>
<td></td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td></td>
<td>+4V to +7V</td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%; TA = Industrial or Military

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>20% VCC</td>
<td>V</td>
<td>0V ≤ VIN ≤ VCC</td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>μA</td>
<td>IOH = -6.0mA, E1 = E2 = Low</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>VCC -0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>0.4</td>
<td>V</td>
<td>IOH = -9.0mA, E1 = E2 = Low</td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-10</td>
<td>10</td>
<td>μA</td>
<td>0V ≤ VO ≤ VCC, E1 = E2 = High</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>10</td>
<td>μA</td>
<td>VIN = VCC or GND, VCC = 5.5V</td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>Input Capacitance*</td>
<td>5</td>
<td>pF</td>
<td>VIN = 0V; TA = 25°C; f = 1MHz</td>
<td></td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance*</td>
<td>15</td>
<td>pF</td>
<td>VIN = 0V; TA = 25°C; f = 1MHz</td>
<td></td>
</tr>
</tbody>
</table>

* Guaranteed and sampled, but not 100% tested.

CL = 300pF

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPD</td>
<td>Propagation Delay</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tEN</td>
<td>Enable Time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDIS</td>
<td>Disable Time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tSET</td>
<td>Input Setup Time</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tHOLD</td>
<td>Input Hold Time</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tpw</td>
<td>Pulse Width</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tR</td>
<td>Output Rise Time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tF</td>
<td>Output Fall Time</td>
<td>35</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRESET</td>
<td>Reset Delay Time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

VCC = 5.0V
TEMP. = 25°C
Switching Waveforms

Switching Waveforms

\[ \begin{align*}
\text{\textit{L}} & \quad \text{TICT} & \quad \text{TICT} \\
\text{\textit{A}} & \quad \text{\textit{S}} & \quad \text{\textit{S}} \\
\text{\textit{Y}} & \quad \text{\textit{O}} & \quad \text{\textit{O}}
\end{align*} \]

\[ \text{E} = \text{LOW} \]

\[ \begin{align*}
\text{\textit{E}} & \quad \text{TICT} & \quad \text{TICT} \\
\text{\textit{Y}} & \quad \text{TICT} & \quad \text{TICT} \\
\text{\textit{R}} & \quad \text{TICT} & \quad \text{TICT}
\end{align*} \]

All inputs have \( t_R, t_F \leq 20\text{ns} \).

OUTPUT TEST CIRCUIT FOR PROPAGATION DELAYS

OUTPUT TEST CIRCUIT FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on \( V_{\text{CC}} \), which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1\mu F ceramic disk decoupling capacitor be placed between \( V_{\text{CC}} \) and GND at each device to filter out this noise.

PROPA GATION DELAYS

![Typical Curves](image)

TYPICAL CURVES
HD-6435
CMOS HEX RESETTABLE LATCHED BUS DRIVER

**Features**

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY ........................................... 300pF
- SOURCE CURRENT .......................................... 6mA
- SINK CURRENT ............................................. 9mA
- PROPAGATION DELAY ........................................ 45nsec @ 5V

**Description**

The HD-6435 is a self-aligned silicon gate CMOS latching Three State bus driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A low on both strobe lines (L) allows data to go through the latches and a transition to high latches the data. A high on either Three State control (E) forces the buffers to the high impedance mode without disturbing the latched data. A low on either reset line (R) forces each of the latches to a low level. New data may be latched in while the buffers are in the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

**Pinout**

<table>
<thead>
<tr>
<th>PIN</th>
<th>TOP VIEW</th>
</tr>
</thead>
<tbody>
<tr>
<td>3Y</td>
<td>VCC</td>
</tr>
<tr>
<td>2Y</td>
<td>19 YY</td>
</tr>
<tr>
<td>1Y</td>
<td>18 YY</td>
</tr>
<tr>
<td>1A</td>
<td>17 YY</td>
</tr>
<tr>
<td>2A</td>
<td>16 YA</td>
</tr>
<tr>
<td>3A</td>
<td>15 YA</td>
</tr>
<tr>
<td>R1</td>
<td>14 A1</td>
</tr>
<tr>
<td>R2</td>
<td>13 A2</td>
</tr>
<tr>
<td>E1</td>
<td>9 E1</td>
</tr>
<tr>
<td>GND</td>
<td>10 E2</td>
</tr>
</tbody>
</table>

**Truth Table**

<table>
<thead>
<tr>
<th>CONTROL INPUTS</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1, R2, E1, E2</td>
<td>A, Y</td>
</tr>
<tr>
<td>X, X, H, X, X, X</td>
<td>X, Hi-Z</td>
</tr>
<tr>
<td>X, X, H, X, X, X</td>
<td>X, Hi-Z</td>
</tr>
<tr>
<td>L, X, L, L, X, X</td>
<td>X, L</td>
</tr>
<tr>
<td>X, L, L, L, X, X</td>
<td>X, L</td>
</tr>
<tr>
<td>X = Don't Care</td>
<td></td>
</tr>
<tr>
<td>H = High</td>
<td></td>
</tr>
<tr>
<td>† = Transition from a Low to High level</td>
<td></td>
</tr>
</tbody>
</table>

**Functional Diagram**
### Specifications HD-6435

#### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td></td>
<td>+8.0V</td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6435-9</td>
<td></td>
<td>-65°C</td>
<td>+150°C</td>
</tr>
<tr>
<td>Military HD-6435-2</td>
<td></td>
<td>-40°C</td>
<td>+85°C</td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td></td>
<td>+4V</td>
<td>+7V</td>
</tr>
</tbody>
</table>

#### ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical “1” Input Voltage</td>
<td>70% VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logical “0” Input Voltage</td>
<td>20% VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IIL</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>µA</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical “1” Output Voltage</td>
<td>VCC -0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Logical “0” Output Voltage</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-10</td>
<td>10</td>
<td>µA</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>10</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>Input Capacitance*</td>
<td>5</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance*</td>
<td>15</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

**D.C.**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPD</td>
<td>Propagation Delay</td>
<td>45</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tEN</td>
<td>Enable Time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDIS</td>
<td>Disable Time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tSET</td>
<td>Input Setup Time</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tHOLD</td>
<td>Input Hold Time</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tPW</td>
<td>Pulse Width</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tR</td>
<td>Output Rise Time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tF</td>
<td>Output Fall Time</td>
<td>35</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tRESET</td>
<td>Reset Delay Time</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

* Guaranteed and sampled, but not 100% tested.

**A.C.**

| Symbol | Parameter                        | Min     | Max     | Units |

#### TEST CONDITIONS

- **VCC = 5.0V ± 10%; TA = Industrial or Military**
- **CL = 300pF**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>5.0V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TEMP. = 25°C**
Switching Waveforms

\[ t_{PW}; t_{SET}; t_{HOLD}; t_{PD}; t_{RESET} \]

All inputs have \( t_R, t_F \leq 20\text{ns} \).

OUTPUT TEST CIRCUIT FOR PROPAGATION DELAYS

OUTPUT TEST CIRCUIT FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on \( V_{CC} \), which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1\( \mu \)F ceramic disk decoupling capacitor be placed between \( V_{CC} \) and GND at each device to filter out this noise.

PROPAGATION DELAYS

\[ t_{PD} \]

\[ t_{PD} (300\text{pF}) \]

\[ t_{R}, t_{F} \]

\[ t_{R}, t_{F} (300\text{pF}) \]

FIGURE 1

FIGURE 2

TYPICAL CURVES

4-37
Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY: 300pF
- SOURCE CURRENT: 6mA
- SINK CURRENT: 9mA
- PROPAGATION DELAY: 45nsec @ 5V

Description

The HD-6436 is a self-aligned silicon gate CMOS Three State buffer driver. The circuit consists of 8 non-inverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three State control line E1 or E2 will force the drivers to the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

<table>
<thead>
<tr>
<th>CONTROL INPUTS</th>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>E1  E2</td>
<td>A</td>
<td>Y</td>
</tr>
<tr>
<td>L  L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L  L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L  H</td>
<td>X</td>
<td>Hi-Z</td>
</tr>
<tr>
<td>H  L</td>
<td>X</td>
<td>Hi-Z</td>
</tr>
<tr>
<td>H  H</td>
<td>Hi-Z</td>
<td>Hi-Z</td>
</tr>
</tbody>
</table>

L = Low, H = High
X = Don’t Care
Hi-Z = High Impedance

Functional Diagram
**Specifications HD-6436**

### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td></td>
<td></td>
<td>+8.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V to VCC +0.3V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td>-65°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td>+150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Industrial HD-6436-9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Military HD-6436-2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### ELECTRICAL CHARACTERISTICS

\[ V_{CC} = 5.0V \pm 10\%; \; T_A = \text{Industrial or Military} \]

#### D.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH} )</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td>V</td>
<td>V</td>
<td>0V \leq V_{IN} \leq V_{CC}</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>20% VCC</td>
<td>V</td>
<td>( I_{OL} = 6.0mA )</td>
<td></td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>( \mu A )</td>
<td>( E_1 = E_2 = \text{Low} )</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>VCC -0.4</td>
<td>V</td>
<td>( I_{OH} = 9.0mA )</td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>0.4</td>
<td>V</td>
<td>( \mu A )</td>
<td>( 0V \leq V_{O} \leq V_{CC} ),</td>
</tr>
<tr>
<td>( I_{O} )</td>
<td>Output Leakage</td>
<td>-10</td>
<td>10</td>
<td>( \mu A )</td>
<td>( E_1 = E_2 = \text{High} )</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Supply Current</td>
<td>10</td>
<td>( \mu A )</td>
<td>( V_{IN} = V_{CC} )</td>
<td></td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance*</td>
<td>5</td>
<td>( pF )</td>
<td>( V_{IN} = 0V; ; T_A = 25°C; )</td>
<td></td>
</tr>
<tr>
<td>( C_{O} )</td>
<td>Output Capacitance*</td>
<td>15</td>
<td>( pF )</td>
<td>( V_{IN} = 0V; ; T_A = 25°C; )</td>
<td></td>
</tr>
</tbody>
</table>

* Guaranteed and sampled, but not 100% tested.

\[ C_L = 300pF \]

#### A.C.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{PD} )</td>
<td>Propagation Delay</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{EN} )</td>
<td>Enable Time</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{DIS} )</td>
<td>Disable Time</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{R} )</td>
<td>Output Rise Time</td>
<td>40</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{F} )</td>
<td>Output Fall Time</td>
<td>35</td>
<td>ns</td>
</tr>
</tbody>
</table>

\[ V_{CC} = 5.0V \]

\[ \text{TEMP.} = 25°C \]
Switching Waveforms

A

\[ \begin{align*}
\text{E}_1 = \text{E}_2 = \text{LOW} \\
50\% \quad \text{tPD} \quad 90\% \quad 10\%
\end{align*} \]

Y

\[ \begin{align*}
\bar{E} \\
50\% \quad \text{tEN} \quad 60\% \quad \text{tDIS} \quad 90\% \\
40\% \\
10\%
\end{align*} \]

All inputs have \( t_R, t_F \leq 20\text{ns} \).

OUTPUT TEST CIRCUIT FOR PROPAGATION DELAYS

OUTPUT TEST CIRCUIT FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The instantaneous current required to switch a large capacitance load may cause a voltage spike on \( \text{VCC} \), which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1\( \mu \)F ceramic disk decoupling capacitor be placed between \( \text{VCC} \) and GND at each device to filter out this noise.

PROPAGATION DELAYS

\[
\begin{align*}
&\text{tPD} \\
\frac{\text{tPD}}{\text{tPD (300pF)}} &\leq 1.24 \\
&1.16 \\
&1.08 \\
&1.00 \\
&0.92 \\
&0.84 \\
&0.76 \\
&0.68
\end{align*}
\]

\[
\begin{align*}
&\text{tR, tF} \\
\frac{\text{tR, tF}}{\text{tR, tF (300pF)}} &\leq 1.8 \\
&1.6 \\
&1.4 \\
&1.2 \\
&1.0 \\
&0.8 \\
&0.6 \\
&0.4 \\
&0.2
\end{align*}
\]

FIGURE 1

FIGURE 2

TYPICAL CURVES
**HD-6440**

**CMOS LATCHED 3 TO 8 LINE DECODER-DRIVER**

### Features
- HIGH SPEED DECODING FOR MEMORY ARRAYS
- INCORPORATES 3 ENABLE INPUTS TO SIMPLIFY EXPANSION
- LOW POWER ............... TYPICALLY<50\mu \text{W} @ 5V STANDBY
- HIGH NOISE IMMUNITY
- AVAILABLE IN BOTH MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- HIGH CAPACITANCE DRIVE ................................ 200pF
- HIGH OUTPUT DRIVE ....................................... \( I_{OH} = -2mA, I_{OL} = 2.4mA \)
- SINGLE POWER SUPPLY

### Description

The HD-6440 is a self aligned silicon gate latched decoder. One of 8 output lines is decoded, and brought to a low state, from the 3 input lines. There are two latch enables (L1, L2), one complemented and one not, to eliminate the need for external gates. The output is enabled by three different output enables (G1, G2, G3), two of them complemented and one not. Each output remains in a high state until it is selected, at which time it will go low.

When using high speed CMOS memories, the delay time of the HD-6440 and the enable time of the memory is usually less than the access time of the memory. This assures that memory access time will not be lengthened by the use of the HD-6440 latched decoder driver. The latch is useful for memory mapping or for systems which use a multiplexed bus.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

### Truth Table

<table>
<thead>
<tr>
<th>ENABLE ADDRESS</th>
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Specifications HD-6440A

ABSOLUTE MAXIMUM RATINGS

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<th>Parameter</th>
<th>Min</th>
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<th>Units</th>
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<td>12.0V</td>
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<td>Input or Output Voltage Applied</td>
<td>GND -0.3V</td>
<td>Vcc +0.3</td>
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<tr>
<td>Storage Temperature Range</td>
<td>-65°C</td>
<td>+150°C</td>
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<tr>
<td>Operating Temperature Range</td>
<td>-40°C</td>
<td>+85°C</td>
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<tr>
<td>Industrial HD-6440A-9</td>
<td>-55°C</td>
<td>+125°C</td>
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<tr>
<td>Military HD-6440A-2</td>
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<tr>
<td>Operating Voltage Range</td>
<td>+4 to</td>
<td>+11V</td>
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ELECTRICAL CHARACTERISTICS

VCC = 10V ± 10%; TA = Industrial or Military

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<th>SYMBOL</th>
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<th>MAX</th>
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<th>TEST CONDITIONS</th>
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<tbody>
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<td>VIH</td>
<td>Logical “1” Input Voltage</td>
<td>70% VCC</td>
<td>V</td>
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<td>VCC - 0.4</td>
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<tr>
<td>VIL</td>
<td>Logical “0” Input Voltage</td>
<td>20% VCC</td>
<td>V</td>
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<td>V</td>
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<tr>
<td>IL</td>
<td>Input Leakage</td>
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<td>µA</td>
<td>IOH = -5.0mA</td>
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<td>VOH</td>
<td>Logical “1” Output Voltage</td>
<td>VCC</td>
<td>V</td>
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<td>IOH = -5.0mA</td>
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<td>VOL</td>
<td>Logical “0” Output Voltage</td>
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<td>V</td>
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<td>IOL = 5.0mA</td>
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<td>ICC</td>
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<td>100</td>
<td>µA</td>
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<td>VCC = 11V</td>
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<td>CIN</td>
<td>Input Capacitance*</td>
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<td>15</td>
<td>pF</td>
<td>VIN = 0V; TA = 25°C; f = 1MHz</td>
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<tr>
<td>CO</td>
<td>Output Capacitance*</td>
<td></td>
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D.C.

*Guaranteed and sampled, but not 100% tested.

A.C.

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<thead>
<tr>
<th>SYMBOL</th>
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<td>Input Hold Time</td>
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<td>Output Rise Time</td>
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<td>tF</td>
<td>Output Fall Time</td>
<td>45</td>
<td>60</td>
<td>ns</td>
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NOTE: All devices guaranteed at worse case limits. Room temperature, 10V data provided for information - not guaranteed.
Specifications HD-6440

**ABSOLUTE MAXIMUM RATINGS**

<table>
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<th>Parameter</th>
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<th>Units</th>
<th>Test Conditions</th>
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<tbody>
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<td>Supply Voltage</td>
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<td>Input or Output Voltage Applied</td>
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<td>GND -0.3V to VCC +0.3</td>
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<tr>
<td>Storage Temperature Range</td>
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<td></td>
<td>-65°C to +150°C</td>
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<tr>
<td>Operating Temperature Range</td>
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</tr>
<tr>
<td>Industrial HD-6440A-9</td>
<td></td>
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<td>-40°C to +85°C</td>
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<td>Military HD-6440A-2</td>
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<td>-55°C to +125°C</td>
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<tr>
<td>Operating Voltage Range</td>
<td></td>
<td>+4 to +7V</td>
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**ELECTRICAL CHARACTERISTICS**

\[ V_{CC} = 5.0V \pm 10\%; \; T_A = \text{Industrial or Military} \]

<table>
<thead>
<tr>
<th>Symbol</th>
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<th>Test Conditions</th>
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<tr>
<td></td>
<td><strong>VCC = 5.0V ± 10%; ; T_A = \text{Industrial or Military}</strong></td>
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<tr>
<td></td>
<td><strong>VCC = 5.0V</strong></td>
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<td></td>
<td><strong>25°C</strong></td>
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<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>70% VCC</td>
<td>20% VCC</td>
<td>V</td>
<td>0V \leq V_{IN} \leq VCC</td>
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<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>VCC - 0.4</td>
<td>0.4 V</td>
<td>V</td>
<td>i_{OH} = 2.4mA</td>
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<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>10 μA</td>
<td>10 μA</td>
<td>μA</td>
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<td>CIN</td>
<td>Input Capacitance*</td>
<td>5 pF</td>
<td>15 pF</td>
<td>pF</td>
<td>V_{IN} = 0V; ; T_A = 25°C; f = 1MHz</td>
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<tr>
<td>CO</td>
<td>Output Capacitance*</td>
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*Guaranteed and sampled, but not 100% tested.

\[ V_{ce} = 5.0V \pm 10\% \]

\[ V_{dc} = 5.0V \pm 10\% \]

\[ T_A = \text{Indust. or Mil.} \]

**A.C.**

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<td><strong>CL = 200pF</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>VCC = 5.0V</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>25°C</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>TA = \text{Indust. or Mil.}</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1SET</td>
<td>Input Setup Time</td>
<td>20</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>tHOLD</td>
<td>Input Hold Time</td>
<td>20</td>
<td>20</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>1PD</td>
<td>Propagation Delay</td>
<td>65</td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>1EN</td>
<td>Enable Time</td>
<td>50</td>
<td>80</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>1DIS</td>
<td>Disable Time</td>
<td>50</td>
<td>90</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>1PW</td>
<td>Pulse Width</td>
<td>30</td>
<td>30</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>1R</td>
<td>Output Rise Time</td>
<td>60</td>
<td>90</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>1F</td>
<td>Output Fall Time</td>
<td>50</td>
<td>80</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTE:**

All devices guaranteed at worst case limits. Room temperature, 10V data provided for information - not guaranteed.
**Switching Waveforms**

![Waveform Diagram]

All Inputs have \( t_{R} \), \( t_{F} < 20 \text{ns} \)

OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

---

**DECOUPLING CAPACITORS**

The Transient current required to charge the load capacitance is given by

\[
I_T = C \frac{dV}{dt}
\]

Assuming that all outputs may change state at the same time and that \( \frac{dV}{dt} \) is constant; \( I_T = \left( \sum C_L \right) \frac{V_{CC} \times 80\%}{t_{R} \text{ or } t_{F}} \)

Let \( C_L = 200 \text{pF} \), \( I_T = (2) (200 \times 10^{-12}) \frac{5.0 \times 0.8}{60 \times 10^{-9}} = 26.7 \text{mA} \)

This current spike may cause a large negative voltage spike on \( V_{CC} \), which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 \( \mu \text{F} \) ceramic disk decoupling capacitor be placed between \( V_{CC} \) and GND at each device to filter out this noise.

---

**PROPAGATION DELAY**

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of \( \pm 10\% \), an ambient temperature of as high as 125\(^\circ\)C, and a calculated load capacitance of 150pF. This application requires the HD-6440-2. The table of A.C. specs shows the \( t_{PD} \) at 4.5V and 125\(^\circ\)C is 100nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.97. The adjusted propagation delay, to the 10% or 90% point, is therefore 100 x 0.97 or 97nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125\(^\circ\)C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.85. The adjusted rise time is, therefore, 90 x 0.85 or 76.5nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 135nsec. The rise time was used here because it is always the worst case.
Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY: 300pF
- SOURCE CURRENT: 4mA
- SINK CURRENT: 6mA
- PROPAGATION DELAY: 35nsec @ 5V

Description

The HD-6495 is a self aligned silicon gate CMOS Three-State buffer driver. The circuit consists of 6 non-inverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three-State control line $E_1$ or $E_2$ will force the drivers to the high impedance mode.

Outputs guaranteed valid at VCC 2.0V for Battery Backup Applications.

Truth Table

<table>
<thead>
<tr>
<th>CONTROL INPUTS</th>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_1$</td>
<td>$E_2$</td>
<td>$A$</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>X</td>
</tr>
</tbody>
</table>

$X =$ DON'T CARE
HI-Z = HIGH IMPEDANCE

Functional Diagram
Specifications HD-6495A

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+12.0V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td>GND -0.3V to VCC +0.3V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>Industrial HD-6495A-9</td>
<td>-40°C to +85°C</td>
<td></td>
</tr>
<tr>
<td>Military HD-6495A-2</td>
<td>-55°C to +125°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Voltage Range</td>
<td>+4 to +11V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

\[ V_{CC} = 10V \pm 10\%; T_A = \text{Industrial or Military} \]

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IH} )</td>
<td>Logical &quot;1&quot; Input Voltage</td>
</tr>
<tr>
<td>( V_{IL} )</td>
<td>Logical &quot;0&quot; Input Voltage</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input Leakage</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Logical &quot;1&quot; Output Voltage</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Logical &quot;0&quot; Output Voltage</td>
</tr>
<tr>
<td>( I_O )</td>
<td>Output Leakage</td>
</tr>
<tr>
<td>( I_{CC} )</td>
<td>Supply Current</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input Capacitance*</td>
</tr>
<tr>
<td>( C_O )</td>
<td>Output Capacitance*</td>
</tr>
<tr>
<td>( I_{ON} )</td>
<td></td>
</tr>
<tr>
<td>( I_{OL} )</td>
<td></td>
</tr>
<tr>
<td>( t_D )</td>
<td>Propagation Delay</td>
</tr>
<tr>
<td>( t_{EN} )</td>
<td>Enable Time</td>
</tr>
<tr>
<td>( t_{DIS} )</td>
<td>Disable Time</td>
</tr>
<tr>
<td>( t_R )</td>
<td>Output Rise Time</td>
</tr>
<tr>
<td>( t_F )</td>
<td>Output Fall Time</td>
</tr>
</tbody>
</table>

**NOTE** All devices guaranteed at worst case limits. Room temperature, 10V data provided for information—not guaranteed.
Specifications HD-6495

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Volts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td></td>
<td></td>
<td>+8.0V</td>
</tr>
<tr>
<td>Input or Output Voltage Applied</td>
<td></td>
<td></td>
<td>GND -0.3V to VCC +0.3V</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td></td>
<td></td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
<td></td>
<td>-40°C to +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-55°C to +125°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+4 to +7V</td>
</tr>
</tbody>
</table>

ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%; TA = Industrial or Military

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIH</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>70% VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VIL</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>20% VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>III</td>
<td>Input Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>VOH</td>
<td>Logical &quot;1&quot; Output Voltage</td>
<td>VCC -0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>Logical &quot;0&quot; Output Voltage</td>
<td>0.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>Output Leakage</td>
<td>-1.0</td>
<td>1.0</td>
<td>μA</td>
</tr>
<tr>
<td>ICC</td>
<td>Supply Current</td>
<td>10</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>CIN</td>
<td>Input Capacitance*</td>
<td>5</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>CO</td>
<td>Output Capacitance*</td>
<td>15</td>
<td></td>
<td>pF</td>
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</table>

D.C.:

C_L = 300pF

A.C.:

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPD</td>
<td>Propagation Delay</td>
<td>35</td>
<td>45</td>
<td>ns</td>
</tr>
<tr>
<td>tEN</td>
<td>Enable Time</td>
<td>90</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>tDIS</td>
<td>Disable Time</td>
<td>90</td>
<td>100</td>
<td>ns</td>
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<tr>
<td>tR</td>
<td>Output Rise Time</td>
<td>85</td>
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<tr>
<td>tF</td>
<td>Output Fall Time</td>
<td>65</td>
<td>75</td>
<td>ns</td>
</tr>
</tbody>
</table>

NOTE: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information—not guaranteed.
Switching Waveforms

All inputs have \( t_R, t_F \leq 20\text{ns} \).

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by

\[
I_T = C \frac{dv}{dt}
\]

Assuming that all outputs may change state at the same time and that \( \frac{dv}{dt} \) is constant; \( I_T = \left( \sum C_L \right) \left( \frac{V_{CC} \times 80\%}{t_R \text{ or } t_F} \right) \)

\[
C_L = 300\text{pF}, I_T = (6) \left( 300 \times 10^{-12} \right) \frac{5.0 \times 0.8}{85 \times 10^{-9}} = 84.7\text{mA}.
\]

This current spike may cause a large negative voltage spike on \( V_{CC} \), which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 \( \mu \text{F} \) ceramic disk decoupling capacitor be placed between \( V_{CC} \) and GND at each device to filter out this noise.

PRODUCTION DELAYS

The above example will illustrate the calculation of a more useful propagation delay. The system on this example uses a 5 volt supply with a tolerance of \( \pm 10\% \), an ambient temperature of as high as 125\( ^\circ \text{C} \), and a calculated load capacitance of 150pF. This application requires the HD-6495-2. The table of A.C. specs shows the \( t_{PD} \) at 4.5V and 125\( ^\circ \text{C} \) is 45nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 45 \( \times \) 0.84 or 38nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125\( ^\circ \text{C} \) to obtain a worst case rise time of 95nsec. Use Figure 2 to find it’s degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 \( \times \) 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 69nsec. The rise time was used here because it is always the worst case.
<table>
<thead>
<tr>
<th>Support Overview</th>
<th>5–2</th>
</tr>
</thead>
<tbody>
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<td>Support Hardware</td>
<td></td>
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<tr>
<td>HB-61000 MICRO 12 Evaluation Board</td>
<td>5–4</td>
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<tr>
<td>HB-61001 4K x 12 Memory Board</td>
<td>5–8</td>
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<tr>
<td>DECstation-78</td>
<td>5–13</td>
</tr>
<tr>
<td>Support Software</td>
<td>5–17</td>
</tr>
<tr>
<td>Support Literature</td>
<td>5–21</td>
</tr>
<tr>
<td>Introduction to DECUS</td>
<td>5–22</td>
</tr>
</tbody>
</table>
Support Overview

Harris provides the foundation tools needed for system development including a prototyping board and thorough documentation. For software development needs, Harris recommends the use of DIGITAL Equipment Corporation's DECstation-78 because it provides flexibility and versatility for many functions.

The MICRO-12 is an all CMOS, single-board system that can be obtained either fully assembled or in kit form. To complement the MICRO-12, a 4K CMOS RAM board is also available. Both the MICRO-12 and the RAM board have wire-wrap areas available for prototyping specialized interfaces such as A/D converters.

The DECstation-78 is a "packaged" computer system that in its basic configurations comprise an LSI version of the 16K PDP-8 minicomputer, a video display terminal, one or two RX78 Dual Floppy Disk drive(s), an easy-to-use interface system, and a versatile operating software system OS/78. Unlike other systems which must be configured from individually selected system components, DECstation-78's components are carefully matched and tested as a system by DIGITAL to ensure hassle-free startup. Harris offers application software to link the DECstation-78 to the MICRO-12 and to a Data I/O Model 9 PROM Programmer.

The DECstation-78 can be easily programmed to perform in a wide range of data processing environments — everything from personal computing and software development to real-time, multitasking operations and networking. The Operating System OS/78 supports the popular high-level programming languages BASIC and FORTRAN IV and is an excellent tool for general purpose program development in the single user environment.
Installation is simple. There is only one cable between the processor and each peripheral. Fewer complicated electronic and mechanical parts and interconnection cables mean fewer maintenance problems and easier installation. In fact, system interconnection has been so streamlined and simplified that DECstation-78 can be installed by the user in something less than an hour — without special tools. The interconnections are through external plug-in ports which allow the user to adapt or reconfigure DECstation-78 to handle new processing needs as they occur. The I/O connection panel on the back of the processor contains five ports. Two serial EIA RS-232C asynchronous interface ports are suitable for interfacing with terminals and other devices that operate from 50 to 19,200 baud. One port is equipped for modem control. A parallel I/O port for printers and custom interfacing provides bi-directional 12-bit transfers at rates up to 15K words per second. A disk interface port allows connection to RX78 Floppy Disks.

The OS/78 operating system is a complete software development operating system designed to run on DECstation 78. OS/78 is supplied as part of the basic system. In addition to OS/78, a multitasking real-time operating system RTS/8 is optionally available. RTS/8, assembly language based, allows multiple tasks to run concurrently while competing for resources on a fixed priority basis. For small business applications, the COS-310 commercial operating system can be added. Word processing software, WPS-8, can also be added to help with your documentation requirements.
Features

- COMPLETE SINGLE BOARD CMOS MICROCOMPUTER SYSTEM
- INCLUDES CPU, MEMORY, UART AND I/O
- HIGH PERFORMANCE CMOS 12 BIT CPU
- WIDELY USED PDP-8* INSTRUCTION SET
- INTERFACES DIRECTLY WITH TTY/CRT TERMINAL/TAPE CASSETTE
- INTERACTIVE KEYBOARD & DISPLAY
- USER WIREWRAP AREA
- EXTENSIVE CONTROL PANEL MONITOR IN ROM
- LARGE USER SOFTWARE LIBRARY AVAILABLE
- SMALL 5V POWER SUPPLY INCLUDED.

Description

The Harris MICRO-12 is a fully assembled and tested single board CMOS 12 bit microprocessor system. A preprogrammed ROM provides a system monitor, keyboard and display utilities and system diagnostic capabilities.

The MICRO-12 includes an 8 digit LED display and 16 key-keyboard which allows direct program insertion, execution and examination.

The ROM system monitor also provides a Binary Loader and List capability from a TTY. A Kansas City Standard Tape Cassette interface (300 Baud) provides the user with a simple means of loading and storing programs.
The MICRO-12 is a fully assembled and tested 12 bit CMOS microprocessor system. It is compact (8.4" x 11.6") and provides a full compliment of CMOS system components. A system monitor ROM (1K x 12) allows the user to enter his program manually with a 16 key keyboard or through a TTY or tape cassette by using the Binary Loader feature. A standard program memory of 256 words x 12 bit RAM is provided with optional socket space for a full 1K x 12 program memory. The monitor does not use any of the user program memory.

The system monitor provides the user with four (4) independent breakpoints for program debug. An 8 digit display allows inspection of the address, memory and register data.

A special function key allows the user program to be listed on either an external TTY or CRT. Another special function key allows the user to punch a program tape on the TTY. The Binary Punch feature may also be used to load an external tape cassette from program memory. A 300 baud Kansas City Standard interface is provided for this purpose. Communications rate of 50 to 9600 baud are jumper selectable on the Bit Rate Generator through the Universal Asynchronous Receiver Transmitter (UART).

**KEYBOARD MONITOR COMMANDS:**
- **EXAMINE** — Allow user to inspect memory data at keyed in address.
- **DEPOSIT** — Alters data at data address.

**FUNCTION COMMANDS:**
- **BINARY LOAD** — Allows TTY reader or cassette entry of user program.
- **BINARY PUNCH** — Allows TTY punching or cassette loading of users program.
- **OCTAL LISTING** — Allows TTY printing of user program.
- **BREAKPOINT SET** — Examine/alter any of four software breakpoints.

Documentation package includes detailed information on using the control panel, how the system operates and users manual which contains circuit diagrams and a listing of the control panel program. Several hardware and software examples are included. The Micro-12 User Manual can be ordered from Harris for more detailed information.

**Functional Block Diagram**

![Functional Block Diagram](image)
The HM-6100 CMOS Microprocessor is a single address, fixed word length, parallel transfer 12 bit microprocessor. It is a member of a broad based CMOS product line which comprises 6100 peripheral devices, RAMs, PROMs, ROMs and a full logic family. The processor recognizes the PDP-8" instruction set and utilizes two's complement arithmetic logic. The device is completely static and may be operated from DC to its rated frequency. No external clock generators or controllers are required.

The support chips, Peripheral Interface Element (PIE), Universal Asynchronous Receiver Transmitter (UART), Bit Rate Generator, Read Only Memories (ROM), Random Access Memories (RAM) and Programmable Read Only Memories (PROM) are completely compatible with the microprocessor. All devices are available in either an industrial or a military temperature range.


### Table of Instruction Set

#### BASIC INSTRUCTIONS

<table>
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<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td>7000</td>
<td>No operation</td>
</tr>
<tr>
<td>IAC</td>
<td>7001</td>
<td>Increment accumulator</td>
</tr>
<tr>
<td>RAL</td>
<td>7004</td>
<td>Rotate accumulator left</td>
</tr>
<tr>
<td>RTL</td>
<td>7006</td>
<td>Rotate two left</td>
</tr>
<tr>
<td>RAR</td>
<td>7010</td>
<td>Rotate accumulator right</td>
</tr>
<tr>
<td>RTR</td>
<td>7012</td>
<td>Rotate two right</td>
</tr>
<tr>
<td>BSW</td>
<td>7002</td>
<td>Byte swap</td>
</tr>
<tr>
<td>CML</td>
<td>7004</td>
<td>Complement link</td>
</tr>
<tr>
<td>CMA</td>
<td>7040</td>
<td>Complement accumulator</td>
</tr>
<tr>
<td>CIA</td>
<td>7041</td>
<td>Complement and increment accumulator</td>
</tr>
<tr>
<td>CLL</td>
<td>7100</td>
<td>Clear link</td>
</tr>
<tr>
<td>CLL RAL</td>
<td>7104</td>
<td>Clear link-rotate accumulator, left</td>
</tr>
<tr>
<td>CLL RTL</td>
<td>7106</td>
<td>Clear link-rotate two left</td>
</tr>
<tr>
<td>CLL RAR</td>
<td>7110</td>
<td>Clear link-rotate accumulator, right</td>
</tr>
<tr>
<td>CLL RTR</td>
<td>7112</td>
<td>Clear link-rotate two right</td>
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<td>STL</td>
<td>7120</td>
<td>Set the link</td>
</tr>
<tr>
<td>CLA</td>
<td>7200</td>
<td>Clear accumulator</td>
</tr>
<tr>
<td>CLA IAC</td>
<td>7201</td>
<td>Clear accumulator, increment accumulator</td>
</tr>
<tr>
<td>GLK</td>
<td>7204</td>
<td>Clear link</td>
</tr>
<tr>
<td>CLA CLL</td>
<td>7300</td>
<td>Clear accumulator-clear link</td>
</tr>
<tr>
<td>STA</td>
<td>7240</td>
<td>Set the accumulator</td>
</tr>
</tbody>
</table>

#### GROUP 1 OPERATE MICROINSTRUCTIONS

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>OPERATION</th>
<th>LOG SEQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td>7400</td>
<td>No operation</td>
<td>1</td>
</tr>
<tr>
<td>HLT</td>
<td>7402</td>
<td>Halt</td>
<td>3</td>
</tr>
<tr>
<td>OSR</td>
<td>7404</td>
<td>Or with switch register</td>
<td>3</td>
</tr>
<tr>
<td>SKP</td>
<td>7410</td>
<td>Skip</td>
<td>1</td>
</tr>
<tr>
<td>SNL</td>
<td>7420</td>
<td>Skip on non-zero link</td>
<td>1</td>
</tr>
<tr>
<td>SZL</td>
<td>7430</td>
<td>Skip on zero link</td>
<td>1</td>
</tr>
<tr>
<td>SZA</td>
<td>7440</td>
<td>Skip on zero accumulator</td>
<td>1</td>
</tr>
<tr>
<td>SNA</td>
<td>7450</td>
<td>Skip on non-zero accumulator</td>
<td>1</td>
</tr>
<tr>
<td>SZA SNL</td>
<td>7460</td>
<td>Skip on non-zero accumulator, or skip on non-zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>SNA SZL</td>
<td>7470</td>
<td>Skip on non-zero accumulator, and skip on zero link</td>
<td>1</td>
</tr>
<tr>
<td>SMA</td>
<td>7500</td>
<td>Skip on minus accumulator</td>
<td>1</td>
</tr>
<tr>
<td>SPA</td>
<td>7510</td>
<td>Skip on positive accumulator</td>
<td>1</td>
</tr>
<tr>
<td>SMA SNL</td>
<td>7520</td>
<td>Skip on minus accumulator, or skip on non-zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>SPA SZL</td>
<td>7530</td>
<td>Skip on positive accumulator, and skip on zero link</td>
<td>1</td>
</tr>
<tr>
<td>SMA SZA</td>
<td>7540</td>
<td>Skip on zero accumulator, or skip on non-zero accumulated, or skip on non-zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>SPA SNA</td>
<td>7550</td>
<td>Skip on positive accumulator, or skip on zero accumulated, or skip on non-zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>SMA SZA SNL</td>
<td>7560</td>
<td>Skip on minus accumulator, or skip on zero accumulated, or skip on non-zero link, or skip on zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>SPA SNA SZL</td>
<td>7570</td>
<td>Skip on positive accumulator, and skip on non-zero accumulated, and skip on zero link, or skip on zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>CLA</td>
<td>7600</td>
<td>Clear accumulator</td>
<td>2</td>
</tr>
<tr>
<td>LAS</td>
<td>7604</td>
<td>Load accumulator, with switch register</td>
<td>1,3</td>
</tr>
<tr>
<td>SZA CLA</td>
<td>7640</td>
<td>Skip on zero accumulator, clear accumulator, increment accumulator</td>
<td>1,2</td>
</tr>
<tr>
<td>SNA CLA</td>
<td>7650</td>
<td>Skip on non-zero accumulator, clear accumulator, increment accumulator</td>
<td>1,2</td>
</tr>
<tr>
<td>SMA CLA</td>
<td>7700</td>
<td>Skip on minus accumulator, clear accumulator, increment accumulator</td>
<td>1,2</td>
</tr>
<tr>
<td>SPA CLA</td>
<td>7710</td>
<td>Skip on positive accumulator, clear accumulator, increment accumulator</td>
<td>1,2</td>
</tr>
</tbody>
</table>

#### GROUP 2 OPERATE MICROINSTRUCTIONS

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>OCTAL CODE</th>
<th>OPERATION</th>
<th>LOG SEQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOP</td>
<td>7400</td>
<td>No operation</td>
<td>1</td>
</tr>
<tr>
<td>HLT</td>
<td>7402</td>
<td>Halt</td>
<td>3</td>
</tr>
<tr>
<td>OSR</td>
<td>7404</td>
<td>Or with switch register</td>
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</tr>
<tr>
<td>SKP</td>
<td>7410</td>
<td>Skip</td>
<td>1</td>
</tr>
<tr>
<td>SNL</td>
<td>7420</td>
<td>Skip on non-zero link</td>
<td>1</td>
</tr>
<tr>
<td>SZL</td>
<td>7430</td>
<td>Skip on zero link</td>
<td>1</td>
</tr>
<tr>
<td>SZA</td>
<td>7440</td>
<td>Skip on zero accumulator</td>
<td>1</td>
</tr>
<tr>
<td>SNA</td>
<td>7450</td>
<td>Skip on non-zero accumulator</td>
<td>1</td>
</tr>
<tr>
<td>SZA SNL</td>
<td>7460</td>
<td>Skip on non-zero accumulator, or skip on non-zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>SNA SZL</td>
<td>7470</td>
<td>Skip on non-zero accumulator, and skip on zero link</td>
<td>1</td>
</tr>
<tr>
<td>SMA</td>
<td>7500</td>
<td>Skip on minus accumulator</td>
<td>1</td>
</tr>
<tr>
<td>SPA</td>
<td>7510</td>
<td>Skip on positive accumulator</td>
<td>1</td>
</tr>
<tr>
<td>SMA SNL</td>
<td>7520</td>
<td>Skip on minus accumulator, or skip on non-zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>SPA SZL</td>
<td>7530</td>
<td>Skip on positive accumulator, and skip on zero link</td>
<td>1</td>
</tr>
<tr>
<td>SMA SZA</td>
<td>7540</td>
<td>Skip on zero accumulator, or skip on non-zero accumulated, or skip on non-zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>SPA SNA</td>
<td>7550</td>
<td>Skip on positive accumulator, or skip on zero accumulated, or skip on non-zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>SMA SZA SNL</td>
<td>7560</td>
<td>Skip on minus accumulator, or skip on zero accumulated, or skip on non-zero link, or skip on zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>SPA SNA SZL</td>
<td>7570</td>
<td>Skip on positive accumulator, and skip on non-zero accumulated, and skip on zero link, or skip on zero link, or both</td>
<td>1</td>
</tr>
<tr>
<td>CLA</td>
<td>7600</td>
<td>Clear accumulator</td>
<td>2</td>
</tr>
<tr>
<td>LAS</td>
<td>7604</td>
<td>Load accumulator, with switch register</td>
<td>1,3</td>
</tr>
<tr>
<td>SZA CLA</td>
<td>7640</td>
<td>Skip on zero accumulator, clear accumulator</td>
<td>1,2</td>
</tr>
<tr>
<td>SNA CLA</td>
<td>7650</td>
<td>Skip on non-zero accumulator, clear accumulator</td>
<td>1,2</td>
</tr>
<tr>
<td>SMA CLA</td>
<td>7700</td>
<td>Skip on minus accumulator, clear accumulator</td>
<td>1,2</td>
</tr>
<tr>
<td>SPA CLA</td>
<td>7710</td>
<td>Skip on positive accumulator, clear accumulator</td>
<td>1,2</td>
</tr>
</tbody>
</table>
Specifications

CENTRAL PROCESSOR
HM-6100
• Crystal Controlled ................. 2.45MHz
• Single Power Supply ................ +5 Volts
• CMOS ................. TTL Compatible

MEMORY
ROM – 1K x 12 Bits Monitor (Resident in control panel memory does not use user address space.)
RAM – 256 x 12 Bits (Expandable to 1K words.)

INTERFACES
SERIAL I/O: 20mA Current Loop TTY
RS-232 (Jumper Selectable)
Baud Rate 50 thru 9600 (Jumper Selectable)
BUS: CMOS Compatible (Dual 22 Pin Connector Provided)
PARALLEL I/O: 12 Bit Input (Optional)
12 Bit Output (Optional)
Large User Wirewrap Area Provided for Additional I/O

SOFTWARE
System monitor provided in ROM with resident keyboard, display and serial output control. Allows user to load, dump and display programs.

LITERATURE (Provided with Micro-12)
• Micro-12 User Manual
• Microprocessor Systems Design Manual
• Introduction to Programming
• Assembly Language Reference Card
• Introduction to DECUS

PHYSICAL CHARACTERISTICS
• Height . . . . . . . . . . . . . . . . . . . . . . . . 8.4 Inches
• Width . . . . . . . . . . . . . . . . . . . . . . . . 11.6 Inches
• Depth . . . . . . . . . . . . . . . . . . . . . . . . 0.75 Inches
• Weight . . . . . . . . . . . . . . . . . . . . . . . . 14 Oz.

ELECTRICAL CHARACTERISTICS
• VCC = . . . . . . . . . . . . . . . . . . . . . . . . (+)5 Volts ±10%
• VTTY = . . . . . . . . . . . . . . . . . . . . . . . . (-)12 Volts ±20%, 30mA
  (Req. only if TTY is connected.)
• ICC = . . . . . . . . . . . . . . . . . . . . . . . . .40mA (System), 160mA (Display)

OPTIONS:
• 1K Memory
• 4K Memory
• Parallel I/O
• Downloader Software
HB-61001
CMOS MEMORY BOARD

Features

- SINGLE SUPPLY, 5V
- ALL CMOS SYSTEM, HIGH NOISE IMMUNITY
- LOW POWER, < 12mW MAXIMUM STANDBY
- DATA RETENTION @ 2 VOLTS
- BUS COMPATIBLE WITH HB-61000 MICROCOMPUTER BOARD

Description

The HB-61001 is a fully assembled and tested all-CMOS memory board, designed to interface directly with the HB-61000 (MICRO-12) single board computer.

The board uses Harris' high performance HM-6543 fully static CMOS RAM's. The HB-61001 comes with either 4K x 12 or 2K x 12 organizations with address selectable by jumper options.

Interfacing the board to other systems is extremely easy, only three (3) control signals and a 12-bit multiplexed address/data bus are needed. See bus signals definition for details. There is no field control logic for extended memory.

A wire wrap area (1.7 x 4”2) with .1” center holes are provided on the board for custom interface circuitry, battery back-up circuitry, etc.

Functional Block Diagram
# Specifications HB-61001

## ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+8.0V</td>
<td></td>
</tr>
<tr>
<td>Applied Input or Output Voltage</td>
<td>GND -0.3V</td>
<td>VCC to +0.3V</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +100°C</td>
<td></td>
</tr>
</tbody>
</table>

## OPERATING RANGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Supply Voltage</td>
<td>VCC 4.5V to 5.5V</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>0°C to +70°C</td>
<td></td>
</tr>
<tr>
<td>Physical Characteristics</td>
<td>4.5” x 7.0” x .6”</td>
<td></td>
</tr>
</tbody>
</table>

## ELECTRICAL CHARACTERISTICS

VCC = 5V ±10%  TA = Operating Range

<table>
<thead>
<tr>
<th>Symbol/Parameter</th>
<th>HB-61001-1</th>
<th>HB-61001-2</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICCSB</td>
<td></td>
<td></td>
<td>mA</td>
<td>VI = VCC or GND</td>
</tr>
<tr>
<td>ICCOP</td>
<td>1.0</td>
<td>1.0</td>
<td>mA</td>
<td>IO = HIZ</td>
</tr>
<tr>
<td>VCCDR</td>
<td>2.0</td>
<td>2.0</td>
<td>mA</td>
<td>f = 125kHz</td>
</tr>
<tr>
<td>ICCDR</td>
<td>1.0</td>
<td>1.0</td>
<td>mA</td>
<td>VCC = 3.0</td>
</tr>
<tr>
<td>VIH</td>
<td>70% VCC</td>
<td>VCC +0.3</td>
<td>V</td>
<td>VI = VCC or GND</td>
</tr>
<tr>
<td>VIL</td>
<td>GND -0.3</td>
<td>20% VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VOL</td>
<td>0.4</td>
<td>0.4</td>
<td>V</td>
<td>IOH = -2.0mA</td>
</tr>
<tr>
<td>IOZ</td>
<td>-1.0</td>
<td>+1.0</td>
<td>µA</td>
<td>GND ≤ VI ≥ VCC</td>
</tr>
<tr>
<td>CI</td>
<td>-20</td>
<td>+20</td>
<td>µA</td>
<td>GND ≤ VO ≥ VCC</td>
</tr>
<tr>
<td>CI/O</td>
<td>15</td>
<td>15</td>
<td>pF</td>
<td>I/O = HIZ</td>
</tr>
<tr>
<td>TAS</td>
<td>25</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TAH</td>
<td>75</td>
<td>165</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TLX</td>
<td>200</td>
<td>200</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TLX</td>
<td>450</td>
<td>575</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TAL</td>
<td>450</td>
<td>575</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TCY</td>
<td>650</td>
<td>775</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TEN</td>
<td>250</td>
<td>250</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDIS</td>
<td>150</td>
<td>150</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDS</td>
<td>130</td>
<td>130</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TDH</td>
<td>50</td>
<td>50</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>TWP</td>
<td>220</td>
<td>220</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

1. Operating current (ICCP) is proportional to operating frequency. Example: Typical ICCP 80mA/MHz.
2. Capacitance sampled and guaranteed but not 100% tested.
3. AC test conditions: Inputs TRISE = TFALL ≤ 100ns; Outputs – 1 TTL load and 100pF.
Installing the HB-61001 in the MICRO-12

BASIC INSTALLATION

To install the HB-61001 memory board in the MICRO-12, first determine the amount of RAM that exists on the CPU board.

If there are 256 words of onboard RAM, and no HD-6440 in U14, installing the HB-61001 is accomplished by removing the jumper from pin 8 to 10 of U14 on the MICRO-12 and replacing it with a jumper from pin 10 to pin 6 of U14. Next plug the memory board into the edge connector with the components facing the keypad.

If there are more than 256 words of RAM and a HD-6440 in U14 on the MICRO-12 replace the jumper from pin 2 to 7 of DSW-1 on the MICRO-12 with one from pin 8 to ground of DSW-1 and plug in the memory board.

SPECIAL HINTS FOR 2K VERSION USERS

It is possible for users of the 2K version (HB-61001-2) to actually have up to 3K of useable read write memory. This is accomplished by utilizing both the MICRO-12 onboard memory and the external memory board. Setting the HB-61001 memory board to reside at locations 2000-5777 octal and leaving the MICRO-12 memory enabled allows the use of all available memory. See the truth table on the first page for details on setting the address of the HB-61001-2. Refer to the MICRO-12 manual, page A-61 for details of the onboard memory circuits.

Battery Back-Up

In many applications it is desirable to provide for data retention during power interruptions. The circuit shown in Figure 3 will provide power to the memory during power outages and doubles as a battery charging circuit during normal operation.

In addition to providing a standby supply, the user must take precautions to guarantee that none of the CMOS inputs are left floating during the power outage. The easiest way to accomplish this, is to add 10K pull-up resistors from all board inputs to CMOS VCC.

FIGURE 2 – HB-61001 Dimensions

FIGURE 3 – A Typical Battery Back-Up Circuit
**Bus Signal Definitions**

(Connector Type: Dual 22 Pin .156” spacing)

<table>
<thead>
<tr>
<th>PIN #</th>
<th>SIGNAL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, A, B</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>2</td>
<td>LXMAR</td>
<td>Chip enable signal; the negative going edge latches address in RAM and initializes a memory cycle.</td>
</tr>
<tr>
<td>3</td>
<td>DX0</td>
<td>Multiplexed address/data bus, most significant bit.</td>
</tr>
<tr>
<td>4</td>
<td>DX1</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>DX2</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>DX3</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>DX4</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>DX5</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>DX6</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>DX7</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>DX8</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>DX9</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>DX10</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>DX11</td>
<td>Multiplexed address/data bus, least significant bit.</td>
</tr>
<tr>
<td>15</td>
<td>XTC</td>
<td>READ/WRITE control signal (READ = High, WRITE = Low)</td>
</tr>
<tr>
<td>16</td>
<td>MEMSEL</td>
<td>Memory select, active low.</td>
</tr>
<tr>
<td>Z, 22</td>
<td>VCC</td>
<td>+5V (± 10%) Supply</td>
</tr>
</tbody>
</table>
In DECstation-78 the computer and terminal are a single compact unit, designated as a VT78 Video Data Processor. The processor and display are interconnected over a high-speed serial line with the processor physically located inside the video display’s case. A single START switch activates the entire system. At system power-up, the display and keyboard are automatically tested.

**VIDEO DISPLAY AND KEYBOARD**

The keyboard/video display is basically a DECscope in origin but has some added features to tailor it to DECstation-78. The same clarity of displayed characters, adjustability of screen intensity, and glare-free screen popular in DECscope products are carried over in DECstation-78. The display system includes a 24-line by 80 character screen format, the complete ASCII upper and lower character set, 33 special symbols, and nineteen user-defined special function keys.

The keyboard is standard typewriter (ANSII) and produces a key-stroke click for audible feedback of key operation. Three-key rollover protection eliminates fast typing errors. Should three keys be depressed simultaneously, transmission will still be correct if one of the first two key typed is released before the third. Note that striking a key does not directly cause a display result. All instructions are fed to the processor which then controls the displayed characters or cursor movements. This is equivalent to a DECscope-Host computer configuration where the instructions are echoed back from the host.

An auxiliary keypad extends the keyboard’s capabilities. The keypad has 19 keys. There are two modes in which the keypad can operate, Normal and Alternate. When in the Normal Mode, the ten numeral keys and the decimal point key, respond like the numeral keys and decimal point key on the main keyboard. The ENTER key responds like the RETURN key. The Alternate Mode is established by an escape sequence (ESC = ) to enter the mode and (ESC > ) to exit the mode. When in the Alternate Mode, the ten numeral keys, the decimal point key, and the ENTER key transmit unique escape codes for custom assignment by the user. In either mode, there are also three blank unassigned keypad keys for user definition. Cursor control keys complete the keypad’s function.
PROCESSOR

The overall organization of DECstation-78 is shown in the Figure below. An LSI (large scale integration) version of the powerful PDP-8 minicomputer contained on a 15 3/4" x 11 7/8" printed circuit board is mounted inside of DECstation-78's video display unit. This is the processor for the system. It includes a 12-bit CPU with memory extension control, 16,384 words (32 bytes) of Random Access Memory, complete peripheral interfacing, internal bootstrap facilities, and a 100Hz real-time clock. The CPU has the same powerful instruction set as the PDP-8A. Cycle time is approximately 3.6 microseconds.

Three general purpose processor registers are provided:

- **PC.** The 12-bit program counter points to the location from which the next instruction will be fetched.
- **AC, L.** The 12-bit accumulator and its 1-bit carry extension, the Link, form the register where all arithmetic calculations take place.
- **MQ.** The 12-bit Multiplier Quotient register serves as a temporary storage register.

Memory

Main memory is 12-bits by 16K words of Random Access NMOS Memory organized as 4 fields of 4K words each. Each field consists of 32 pages of 128 words.

An on-board ROM permits several important features to be included. These are:

- Automatic self-test procedure.
- Processor status display.
- Terminal emulation mode, which allows DECstation-78 to be used as a stand alone computer terminal without independent processing capability.
- Internal disk bootstrap.
- Preselection of baud rates on primary communications port.
Instructions

There are two basic groups of instructions: memory reference and microinstructions. Memory reference instructions require an operand; microinstructions do not. The DECstation-78 processor features indirect addressing capability up to 4K and 8 auto-index registers. Three groups of operate microinstructions perform a variety of program operations without any need for reference to memory location. Groups 1 and 2 allow the programmer to manipulate and/or test the data that is located in the accumulator or link. Group 3 operate instructions allow the programmer to manipulate the MQ register. Many of these operate microinstructions may be combined by the experienced programmer in order to use the DECstation-78 processor more efficiently.

Input/Output (IOT) instructions are used to control the operation of the computer's interrupt system and clock and to make all exchanges of data to the system display, keyboard, and externally connected peripherals.

Interface Ports

There are six interface ports for DECstation-78: a parallel port, a disk interface port, an electronic program injection port and three asynchronous serial ports.

Parallel I/O Port — is for printers and custom interfacing. It provides bi-directional 12-bit transfers at rates up to 15K words per second.

Serial Line Unit-1 (SLU-1) — connects the central processor to the display subsystem internally and is not externally accessible. The two other asynchronous serial EIA RS-232C interface ports are suitable for primary and secondary communications applications, terminals, and the attachment of a variety of devices. These ports (SLU-2 and SLU-3) features 16 program selectable baud rates ranging from 50 to 19,200 baud and programmable loop-back for maintenance. One port, SLU-3, provides programmable parity generation and overrun detection, variable width stop-bit selection and programmable character length. The other port, SLU-2, is equipped for full modem control.

Disk Interface Port — allows connection between the DECstation-78 processor and two independent dual drive disk units (RX78). It provides both 8- and 12-bit data formats for maximum flexibility.

MR78 Electronic Program Injection Port — allows the mounting of an external Read Only Memory program capsule. The MR78 provides high speed loading under control of a pre-programmed ROM unit. Loading is automatically initiated when the DECstation-78 START button is pressed.
RX78 FLOPPY DISK DRIVE

The RX78 Floppy Disk System is an inexpensive mass storage subsystem, I/O and random access file device characterized by speed and reliability. Either one or two compact, self-contained units may be interfaced with the processor via a high-speed data port on the external connector panel.

Track-to-track moves require six milliseconds for the move plus twenty milliseconds for settling time if the head is loaded for a read or write. The rotational speed of the diskette is 360-rpm, with an average latency time of 83 milliseconds. The total average access time is only 263 milliseconds.

The RX78 Floppy Disk System uses IBM-standard diskettes — thin, flexible oxide-coated disks about the size of a 45-rpm phonograph record. The disk is recorded only on one side and is permanently contained in an 8-inch square flexible protective envelope. The diskette contains 77 tracks with 26 sectors per track. Each sector can store 256 8-bit bytes or 128 12-bit words for a total formatted capacity of 512,512 bytes or 256,256 words. The diskette is a portable, convenient storage, interchange and software distribution medium which allows DECstation-78 users to store large amounts of data in a small space.

PRINTERS

For local on-site output, the LA78 DECprinter-1 180-cps line printer is recommended. This printer interfaces via a parallel port on DECstation-78. For word processing applications, the LQP78 letter quality printer is available.
Support Software

Harris supports its microprocessor-based systems through an extensive variety of proven PDP-8 software. For the DECstation-78, there are three major operating system packages available. These are: the OS/78 operating system that is included in the price of the basic DECstation-78 package; an optional commercial operating system, COS-310, for small business applications; and a word processing system, WPS-8, for documentation and other text editing needs. For real-time multitasking, RTS/8 can also be added.

In addition to these basic software support packages, Harris can provide the user application software for linking the DECstation-78 to a hardware development system, such as the MICRO-12. Harris also has a software package to link the DECstation-78 to a Data I/O Model 9 PROM Programmer. PAL-8 based cross assemblers for the popular 8-bit microprocessors can be obtained from various sources, thus increasing the functionality of the DECstation-78. The user also has access to the extensive DECUS library of PDP-8 programs which in many cases can reduce development efforts.

MULTILANGUAGE OPERATING SYSTEM OS/78

OS/78 provides DECstation-78 users with power and flexibility in both interactive and batch programming environments. OS/78 is based on DIGITAL’s proven OS/8 and offers many features previously available only on larger computer systems. OS/78 maximizes utilization of DECstation-78 main memory because the resident portion of the operating system requires only 256 words of memory. Non-resident portions of the system are swapped into memory from the RX78 floppy disk automatically as required.

OS/78 is easy to use and provides the development programmer with a complete, logical interface to program and file structures. All data files and executable programs are stored in one or more floppy disks where they may be accessed for loading, modification or execution by simple keyboard commands.

OS/78 incorporates Commercial BASIC and FORTRAN IV and provides a comprehensive set of software tools and utility programs that help make DECstation-78 an excellent program development and calculations tool in the single-user environment. These include EDIT, PAL8, CREF, ODT and BATCH PROCESSING, among others.
EDIT — is a line-oriented text editor that allows the user to enter and modify ASCII files. It supports commands to list, insert, delete, change and move text as well as to search for character strings.

PAL 8 — is a two-pass language assembler that provides the programmer with the capability of coding directly in machine-oriented symbolic instructions. Its features include: 1) conditional assembly which enables a single source file to produce different binaries for different purposes; 2) paginated listings, page headings and page numbering to improve program documentation; and 3) a symbol table which lists all program labels and their memory location or value.

CREF (Cross-Reference Utility Program) — aids the programmer in writing, debugging and maintaining assembly language programs by providing the ability to pinpoint all references to a particular symbol. CREF provides an alphabetical cross-reference table for PAL8 assembly listings and numbers each line in the listing. Program symbols and literals are printed alphabetically along with the numbers of the lines that reference to them. Optional two-pass operations doubles the number of symbols that can be accommodated in a program.

BITMAP — is an OS/78 utility used to construct a table, or map, showing the memory locations used by a given binary file. BITMAP will accept any absolute binary file as input and route its output to any supported I/O device.

ODT (Octal Debugging Technique) — is invisibly co-resident with the user program so that there is no need to allocate more than 3 words in each 4K field for a debugging package during development. Breakpoints can be set anywhere in a program to allow the programmer to trace the execution of his program. Whenever program execution is suspended, ODT provides the capability to examine and optionally modify memory locations or registers. Specified areas of memory may be searched by means of ODT’s binary memory search mechanism.

OS/78’s Batch Processing utility — allows lengthy sequences of commands or frequently used programs to be run automatically on DECstation-78.

OS/78 BASIC — is high level, easily learned programming language compatible with Dartmouth BASIC. It uses simple English words, abbreviations and familiar mathematical symbols to specify operations. BASIC can be used for executing large data processing tasks as well as performing quick, one-time calculations.

BASIC consists of an editor, compiler, and a runtime system, all three supporting BASIC’s dual functions as an interactive program development tool and a system for interactive and batch execution. The BASIC instruction set includes powerful, yet simply learned commands which allow novices to do useful programming in a relatively short time. Extended operations and functions, such as program chaining and string operations, allow the more experienced programmer to perform intricate manipulations or express a problem efficiently and concisely.

REAL-TIME MULTITASKING RTS/8

RTS/8 allows DECstation-78 to handle many tasks simultaneously by making use of the otherwise idle processor cycles that occur periodically during a program’s execution. A user-defined priority list allows the most important jobs to be processed first. As a result, programs in execution can, if necessary, be temporarily suspended and removed from memory (swapped out) to make room for a higher priority job.

By using RTS/8, the programmer is able to take advantage of a set of software modules that will interface with his hardware, thereby freeing him to concentrate on his own programs and greatly reduce development time. Note: RTS/8 must have OS/78 software as the operating system.
WORD PROCESSING SOFTWARE WPS-8

Word Station 78 is a complete word processing and visual text editing package for use in both stand alone and shared-logic environments. It can be added to the DECstation-78 and includes proven turnkey word processing software. Options include the LQP 78 letter quality printer and a Communications/Optical Character Reader interface which permits the word station to communicate over various grades of communications facilities with host computers or other word stations.

WS78 is powerful yet inexpensive enough to be used as a free-standing word processing system with its own processing capability, local storage and printers. The software is conveniently stored on the system floppy disk. Additional space on the system floppy disk is reserved for a boilerplate library and a shorthand dictionary. “Shorthand” expressions might be names, addresses, titles, technical words or other standard short units of text that an organization uses repeatedly. These expressions may be stored on floppy disk, recalled with a few keystrokes and automatically inserted into the current text, thereby saving hours of retyping and increasing operator productivity. More than one hundred full pages of typing in as many as 200 separate files may be stored on a document diskette.

Because all the “programming” is in the software, DIGITAL word stations can be used by anyone for productive work after only a day’s familiarization with the equipment. A typical stand-alone application, for example, might involve the use a a Word Station 78 in a development facility for the production of reports, documents and correspondence.

Word Station 78 Features:

Software Features:

• “Cue card” prompting of commands via visual display.
• Prestored rulers for margin, printer spacing and tabbing control.
• Format information stored with each document.
• Variety of printer output for mailing labels, envelopes, letterhead, technical manuals, etc.
• Simultaneous printing and editing.
• Justified margins.
• Underlined and overstruck printout.
• Time and date indexing of documents.
• Mailing list generation.
• Form letter merge.
• Insertion of boilerplate material.

Full Editing Features:

• Bi-directional search capabilities.
• Block move (“cut and paste”).
• Editing done by grammatical entities — character, word, tab, column, sentence, line, paragraph, or page.
• Decimal point alignment.
• Swap of transposed characters.
• Manual or automatic pagination.
COMMERCIAL OPERATING SYSTEM COS-310

System Software

DIGITAL's Commercial Operating System (COS-310) is a self-contained, disk-resident operating system for small to medium-sized commercial applications. System features include:

- A comprehensive business programming language, DIGITAL’s Business-Oriented Language (DIBOL).
- Numerous utilities to simplify program development and create, update, sort/merge and back-up data files.
- Sequential or random file accessing from disk storage.
- User file directories.
- A large system message library.
- Multivolume file support.
- Batch and interactive data processing.

Applications Flexibility

One of the most important characteristics designed and built into DEC COS-310 is flexibility — flexibility that lets 310 tackle a wide range of data processing problems and produce solutions quickly, efficiently, and economically. COS-310’s flexibility is shown in its many uses:

- A stand-alone computer system.
- A remote job entry station.
- A “brilliant” terminal functioning as a satellite to a central computer system but having its own totally independent power.

COS-310 also services a wide range of users. Small companies can use COS-310 as their total processing system to perform payroll and other necessary accounting functions. Larger companies can use several DECstation-78’s with COS-310 to decentralize their data processing by placing a DECstation-78 at each branch office to handle remote job entry while providing complete formatting and batch processing capabilities on a local level. Banks, insurance companies, manufacturers, warehousing operations — these are just a few of the many users who can profit from the cost-effective performance of COS-310. Standard applications programs are available from DEC as well as from numerous software firms.

The System for Small Companies

In small companies, COS-310 can be used in many applications areas — from order entry and inventory control to accounts payable, accounts receivable, and payroll. It can maintain credit files and information on outstanding orders, accept order entry information keyed in at the video terminal, print the packing tickets, update the inventory file, and generate invoices. COS-310 can also be used to report on back orders and future orders, to describe the company’s overall sales picture, to keep track of salesmen’s commissions, and to perform sales analysis and related processing tasks.

COS-310 can provide small companies with immediate information when it is needed, not sometime later when the "crisis" has passed. Customers are happier because their orders can be filled faster and more accurately. They receive up-to-date billing information and account statements with no delays — a benefit that means a good cash flow back from customers who want to maintain their credit ratings and/or discounts. Special discounts are easily handled by the system with each customer’s account reflecting information that is unique to that company. Customer orders for the future can be entered into COS-310 and automatically processed at the exact time they were requested.
Support Literature

1. **HARRIS DATA BOOKS**
   - CMOS Microprocessor Data Book
   - Bipolar and CMOS Memory Data Book
   - Analog Data Book

2. **HARRIS MANUALS**
   - Harris Microprocessor Systems Design Manual
   - MICRO-12 User’s Manual

3. **DEC MANUAL**
   - Introduction to Programming

3. **DEC SYSTEM MANUALS**
   - DECstation User’s Guide
   - DECstation Technical Manual
   - OS/78 User’s Manual
   - RTS-8 User’s Manual

**NOTES:**

1. Data Books are available from Harris sales representatives and distributors.

2. Manuals can be purchased from Harris Semiconductor, Melbourne, Fla. (see order form in back of this Data Book.

3. DEC Systems Manuals are available from DIGITAL Equipment Corporation.
Introduction to DECUS™

OVERVIEW

Since the HM-6100 microprocessor was designed to recognize the instruction set of the Digital Equipment Corporation (DIGITAL)™ PDP-8/E™ minicomputer, most programs written for the PDP-8 family are also usable with the HM-6100. The Digital Equipment Computer Users Society (DECUS) provides the vehicle through which HM-6100 and PDP-8 users can exchange ideas, information and user written programs. Harris Semiconductor supports the HM-6100 through participation in the 12-Bit Special Interest Group of DECUS.

HISTORY

DECUS was established in 1961 to "... advance the efficient use of DIGITAL computers. It is a voluntary, not-for-profit users group, supported in part by Digital Equipment Corporation."¹

ACTIVITIES

Symposia

The symposia, which are held throughout the year, provide a forum for users to meet with each other and with DIGITAL management. The papers and presentations are published as DECUS Proceedings shortly after each symposium and provide a permanent record of the meetings activities.

Special Interest Groups (SIGs)

The SIGs promote the interchange of specialized information through the publication of newsletters and the coordination of symposia sessions. At the symposiums they sponsor business meetings, tutorials, and workshops which fulfill the two-fold purpose of fostering communication among users and between users and DIGITAL. User submitted articles, minutes of local meetings, and letters comprise the major portion of the newsletters. Suggestions, hints, bug fixes, program plans, or questions of a non-commercial nature are suitable material for SIG newsletters.

The 12-Bit Special Interest Group is the vehicle through which users interested in 12-Bit hardware and software can share their ideas. Focus on user interest in HM-6100 related material (such as the DECstation-78) is provided by the MICRO-8 Working Group within the 12-Bit SIG. Various application notes, and hardware and software suggestions are covered in the MICRO-8 section of the 12-Bit SIG newsletter and at the symposia.

Program Library

One of the services performed by DECUS is the maintainence of a large library of programs for DIGITAL computers. The DECUS PDP-8 Program Library Catalog lists over 1200 assembly language and FOCAL™ programs organized into 17 categories. Included are text editors, assemblers, debuggers, high-level languages (BASIC, FOCAL, ALGOL, SNOBOL, LISP, etc.), operating systems, input/output device handlers, mathematical packages, and various other types of application software.
MEMBERSHIP

Associate

An individual who wishes to join DECUS is eligible for an Associate (non-voting) membership if he has "...a bonifide interest in DECUS...". Associate Members receive DECUSCOPE, the Society's Newsletter, automatically. They may receive other DECUS material, such as the 12-Bit SIG Newsletter and the PDP-8 Library Catalog, on request.

Installation

An organization, institution, or individual that has purchased, leased, or has on order a computer manufactured by Digital Equipment Corporation (such as a DECstation-78) is eligible for Installation Membership in DECUS.

TM Trademark Digital Equipment Corporation, Maynard, Ma. 01754

1 DECUS Membership Brochure
Harris Reliability & Quality

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Section 2. Reliability Screening Programs 6–10

Section 3. Burn-In Circuits 6–22
Introduction

The Product Assurance Department at Harris Semiconductor Products Division is responsible for assuring that the quality and reliability of all products shipped to customers meets their requirements. During all phases of product fabrication, there are many independent visual and electrical checks performed by Product Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met.

The following military documents provide the foundation for Harris Product Assurance Program.

- MIL-M-38510D “General Specification of Microcircuits”
- MIL-Q-9858A “Quality Program Requirements”
- NASA Publication 200-3 “Inspection System Provisions”
- MIL-C-45662A “Calibration System Requirements”
- MIL-I-4508A “Inspection System Requirements”

The Harris Semiconductor Reliability and Quality Manual, which is available upon request, describes the total function and policies of the organization to assure product reliability and quality. All customers are encouraged to visit the Harris Semiconductor facilities and survey the deployment of the Product Assurance function.

Quality Control

All critical processing steps for digital products are subject to rigid process control monitoring.

For example, to insure process stability of CMOS fabrication, frequent qualification of diffusion furnaces, metallization and passivation equipment by C-V plotting techniques is performed. The C-V plot method provides a very sensitive monitor of the amount of ionic contamination present in the processing equipment, and assures clean process with built-in reliability. Process controls of this kind are one reason Harris products have an excellent reliability record.

Another example, in the case of bipolar memory circuits, is the nichrome fusible link process. This process is rigorously controlled by frequent measurements of parameters such as resistivity and dimensions. Consistent and controlled execution of this process has led to very reliable PROMs of high programmability.

The above are only a few of the many process controls instituted to ensure high quality and reliable products. Some other examples are listed below:

- In-line SEM inspection
- Continuous environmental monitoring for particle count, temperature and humidity
- Oxide and metallization thickness measurements
- Doping concentration and profiles
- Pre and post etch inspections
- Prescribed interval calibration and preventative maintenance of processing equipment
- Total documentation of specifications and change control procedures

The Product Assurance department also maintains a well equipped Analytical Services Department. This area is equipped with a complete electron microscopy laboratory, including Scanning Electron microscopes with energy dispersive x-ray analysis capability, electron microprobe, a Scanning Auger microscope with ESCA attachment, and all sample preparation equipment. The Analytical Services Department also has a complete physical chemistry
laboratory utilized for analyzing the products and process materials for LSI circuits. Equipment in this section includes atomic absorption flame emission spectrometry, arc emission spectrography, gas chromatography, a research grade talstep, an ultraviolet spectrophotometer and an infrared spectrophotometer. This section also contains a complete wet chemical analysis laboratory.

Further, to ensure high quality metal deposition, critical die areas are monitored via in-process SEM.

Reliability

The reliability approach at Harris Semiconductor is based on designing in reliability rather than testing for reliability only. The latter is applied to confirm that sound design with quality and reliability ground rules are observed and correctly executed in a new product design.

Reliability engineering becomes involved as early as concept review of a new product and continues to remain involved through design and layout reviews. At these critical development points of a new design, basic reliability layout guidelines are invoked to insure an all-around reliable design. This concept is reflected by the Harris reliability procedures which encompass mandatory first run product evaluation. This is done at not only the circuit level, but also at the process and package level. Reliability engineering approval is required before new product designs are released to manufacturing.

Both maximum rated and accelerated stress conditions are performed. Acceleration is important to determine how and at what stress level a new design would fail. From this information, necessary design changes can be implemented to insure a wider and safer margin between the maximum rated stress condition and the device’s stress limitation.

The notably low failure rates for all the Harris Semiconductor product lines are a direct result of the application of this reliability concept. Conservatively derating to a typical system condition of +50°C gives a failure rate of 0.020%/1K hrs. for programmed 76XX Bipolar PROMs, a value of 0.013%/1K hrs. for the 65XX CMOS Memory products, and for the CMOS Microprocessor products the rate is 0.015%/1K hrs. The process and layout ground rules are compatible for the Memory and Microprocessor products CMOS lines thus resulting in the expected equivalently low failure rates.

The excellent reliability performance is further exemplified by our customers. Analysis of parts returned to Harris indicates the following results. For the CMOS Microprocessor products and CMOS Memory products, the returns constitute only 0.2% of the total volume shipped.

The accompanying chart illustrates the distribution of categories for why devices are returned. Note that 60-70% of these returned are devices that were not defective as shipped. These units failed due to electrostatic damage (ESD), electrical overstress (EOS), or were good devices which were incorrectly identified as board or system level failures. The latter category is defined as invalid returns and represents 30-40% of the total number of returned units.
Section 1. CMOS Reliability/Quality Enhancement

To ensure a totally reliable product and system, the design engineer needs to understand the capabilities and limitations of the CMOS product. In addition, a clear understanding of the techniques employed to improve reliability is essential for High Reliability system goals. The following describes the necessary tools to enhance CMOS reliability.

DESIGNING OUT FAILURE MODES

Static Charge

Since the introduction of MOS, manufacturers have searched for effective and safe ways of handling this sensitive device. High input impedance of CMOS, coupled with gate-oxide breakdown characteristics, result in susceptibility to electrostatic charge damage.

Figure 1 shows a cross-section of silicon gate MOS structure. Note the very thin oxide layer (~1000Å)* present under the gate material. Actual breakdown voltage for this insulating layer ranges from 70 to 100V.

Handling equipment and personnel, by simply moving, can generate in excess of 10kV of static potential in a low humidity environment. Thus, static voltages, in magnitudes sufficient to damage delicate MOS input gate structures, are generated in most handling environments.

A failure occurs when a voltage of sufficient magnitude is applied across the gate oxide causing it to breakdown and destruct. Molten material then flows into the void creating a short from the gate to the underlying silicon. Such shorts occur either at a discontinuity in doping concentration, or at a defect site in the thin oxide. If no problems appear in the oxide, breakdown would most likely occur at gate/source, or gate/drain intersection coincidence due to the doping concentration gradient.

Noncatastrophic degradation may result due to overstressing a CMOS input. Sometimes an input may be damaged, but not shorted. Most of these failures relate to damage of the protection network, not the gate, and show up as increased input leakage.

*1Å (Angstrom = 10^-8 cm)
Voltage Limiting Input Protection

During the evolution of monolithic MOS, manufacturers developed various protection mechanisms that are an integral part of the circuit. However, several of these earlier techniques have been replaced by improved methods now in use. The object of most of these schemes is to prevent damage to input-gate structures by limiting applied voltages.

Recent CMOS designs employ a dual-diode concept in their input protection networks. Figure 2 illustrates such a protection circuit.

One characteristic of junction-isolated CMOS protection circuits is the ~200Ω current limiting resistor. Cross sectional area of the metallization leading to the resistor, and the area of the resistor are, therefore, designed to absorb discharge energy without sustaining permanent damage. This dual-diode protection has proved very effective and is the most commonly used method in production today.

HARRIS INPUT GATE PROTECTION

To protect input device gates against destructive overstress by static electricity accumulating during handling and insertion of CMOS products, Harris provides a protection circuit on all inputs. The general configuration of this protection circuit is shown in Figure 2.

Both diodes to the VDD and VSS lines have breakdown voltages averaging between 35 and 40 volts. Excessive static charge accumulated on the input pin is thus effectively discharged through these diodes which limit the voltage applied from gate to drain and source. The 200 ohm resistor provides current limiting during discharge. Depending on the polarity of the input static charge and on which of the supply pins is grounded, the protective diodes may either conduct in the forward direction or breakdown in the reverse direction.

In order to test this concept, step stress tests have been performed at Harris using an approximate equivalent circuit to simulate the static charge encountered in handling operations. The equivalent circuit consists of a 100pF capacitor in series with a 1.5K ohm resistor and is considered the rough equivalent of a human body. Step stressing takes the form of charging the capacitor to a given voltage and then discharging it into an input pin of the CMOS device under test according to the sequence given in MIL-STD-38510.

<table>
<thead>
<tr>
<th>Stress Voltage</th>
<th>Cumulative Failures</th>
</tr>
</thead>
<tbody>
<tr>
<td>500</td>
<td>0</td>
</tr>
<tr>
<td>700</td>
<td>0</td>
</tr>
<tr>
<td>1000</td>
<td>0</td>
</tr>
<tr>
<td>1500</td>
<td>1</td>
</tr>
<tr>
<td>1700</td>
<td>3</td>
</tr>
<tr>
<td>1800</td>
<td>4</td>
</tr>
</tbody>
</table>
These results indicate that the input protection used for Harris CMOS products provides adequate protection against static electricity based on the limits specified in MIL-STD-38510.

There are two trade-offs to consider when fabricating an input protection scheme. Effectiveness of the overvoltage protection, and performance of the overall circuit. It is obvious that increasing series resistance and capacitance at an input limits current. This, in turn, increases the input protection's ability to absorb the shock of a static discharge. However, such an approach to protection can have a significant effect on circuit speed and input leakage. The input protection selected must provide a useful performance level and adequate static-charge protection.

Commonly used MOS-input protection circuits all have basic characteristics that limit their effectiveness. The zener diodes, or forward-biased pn-junctions, employed have finite turn-on times too long to be effective for fast rise-time conditions. A static discharge of 1.5kV into a MOS input may bring the gate past its breakdown level before the protection diodes or zener becomes conductive.

Actual turn-on times of zeners and pn-diodes are difficult to determine. It is estimated that they are a few nanoseconds and a few tens of picoseconds, respectively. A low-impedance static source can easily produce rise times equal to or faster than these turn-on times. Obviously the input time constant required to delay buildup of voltage at the gate must be much higher for zener, or other schemes having longer turn-on times.

![Diagram of input protection network](image)

**Figure 2** — Junction isolated dual-diode protection networks are most commonly used in today's CMOS circuits.

Consider an example. Figure 3 shows a test circuit that simulates the discharge of a 1.5kV static charge into a CMOS input. Body capacitance and resistance of the average worker is represented by a 100pF capacitor through 1.5kΩ. Switch A is initially closed, charging 100pF to 1.5kV with switch B open. Switch A is opened, then B is closed, starting the discharge. With the 1.5kΩ x 5pF time constant to limit the charge rate at the DUT input, it would take approximately 350psec to charge to 70V above VDD. Diode turn-on time is much shorter than 350psec, hence the gate node would be clamped before any damage could be sustained.

There is no completely foolproof system of chip-input protection presently in production. If static discharge is of high enough magnitude, or sufficiently short rise-time, some damage or degradation may occur. It is evident, therefore, that proper handling procedures should be adopted.
FIGURE 3 — Input protection network test setup illustrates how diode clamping prevents excessive voltages from damaging the CMOS device.

HANDLING RULES

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Metallic or conductive plastic* tops on work benches connected to ground help eliminate static build-up.

- Ground all handling equipment.

- Ground all handling personnel with a conductive bracelet through 1MΩ to ground. The 1MΩ resistor will prevent injury.

- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold or aid in the generation of a static charge.

- Control relative humidity to as high a level as practical. A higher level of humidity helps bleed away any static charge as it collects.

- Ionized air blowers reduce charge build-up in areas where grounding is not possible or desirable.

- Devices should be in conductive carriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.

- In automated handling equipment, the belts, chutes, or other surfaces the leads contact should be of a conducting nature. If this is not possible, ionized air blowers may be a good alternative.

THE FORWARD–BIAS PHENOMENON

Monolithic CMOS integrated circuits employ a single-crystal silicon wafer into which FET sources and drains are implanted. For complex functions many thousands of transistors may be required and each must be electrically isolated for proper operation.

Junction techniques are commonly used to provide the required isolation — each switching node operating reverse-biased to its respective substrate material. Additionally, as previously mentioned, protection diodes are provided to prevent static-charge related damage where inputs interface to package pins. Forward-biasing any of these junctions with or without power applied may result in malfunction, parametric degradation, or damage to the circuit.

*Supplier: 3M Company "Velostat"
Before proceeding, it should be pointed out that junction isolation, in the classical sense, is not implemented in the CMOS structure. Although commonly called junction isolation, the CMOS technique varies substantially from that used in bipolar TTL (Figure 4).

![Diagram of CMOS Junction Isolation](image)

**FIGURE 4** — Junction isolation for bipolar and CMOS differ considerably. CMOS utilizes a simpler technique that takes advantage of its less complex processing.

**ELECTROMIGRATION AND FUSING**

An aluminum metallization system is used for on-chip interconnect and wire bonding of most CMOS integrated circuits. On-chip metallization means a very pure grade of aluminum deposited on the surface of a silicon wafer. A subsequent metal etch defines the interconnect pattern.

This on-chip metallization can be subject to two primary current-density related failure modes, electromigration and fusing.

Electromigration results from displacement of metal atoms due to high current densities. Displacement of atoms creates physical holes in the metal structure that enlarge with time, eventually causing an open circuit. Under extreme circumstances, displacement can be sufficient to short to an adjacent line. Current density levels for which circuit life is not impaired are subjects of considerable debate. One figure, generally considered to be ultra-safe, is $10^6 \text{A/cm}^2$.

Considerably higher current densities, on the order of $10^6 - 10^8 \text{A/cm}^2$, are required to cause fusing. For a 0.3 mil wide, 40 μ inch thick aluminum line and a fuse current density of $10^7 \text{A/cm}^2$, 775mA will cause fusing. Current levels of this magnitude are not generated during normal CMOS operation.

Could a high-energy static discharge into a CMOS input or output cause fusing? Yes, but such a failure would most likely occur due to heavily forward-biasing an input or output through a low impedance.

High currents resulting from an excessive forward-bias can cause severe overheating localized to the area of a junction. Damage to the silicon, overlying oxide and metallization can result.
BIPOLAR PARASITICS

Care must always be exercised not to forward-bias junctions from input or output pads.

A complex and potential defect phenomenon is the interaction of a npn/pnp combination a la SCR (Figure 5). Forward-biasing the base-emitter junction of either bipolar component can cause the pair to latch-up if $\beta_{\text{npn}} \times \beta_{\text{pnp}} \geq 1$. The resultant low impedance between supply pins can cause fusing of metallization or over-dissipation of the chip.

Figure 5 shows how an SCR might be formed. The p+ diffusion labeled INPUT is connected to aluminum metallization and bonded to a package pin. Biasing this point positive with respect to VDD supplies base drive to the pnp through R2. Although gain of these lateral devices is normally very low, sufficient collector current may be generated to forward-bias and supply substantial base current to the vertical npn parasitic. Once the pair has been activated, each member provides the base current required to sustain the other. A latched condition will be maintained until power is removed or circuit damage disables further operation.

Figure 5 - Improper biasing can latch-up this SCR configuration. A p+ guard ring is commonly used to kill lateral pnp action. This ring is diffused into the surface at the junction of p- and n- silicon.

DESIGN RULES EQUALLY IMPORTANT AS HANDLING RULES

A system using CMOS must have reliability designed in. No amount of testing can guarantee long term reliability when poor design practices are evident.

- Never apply signals to a CMOS circuit before power has been turned on.
- Supply filter capacitance should be distributed such that some filtering is in close proximity to supply pins of each package. Testing has shown 0.01 $\mu$F/package to be effective in filtering noise generated by most CMOS functions.
- CMOS signal lines are terminated at the driving end by a relatively high impedance when operating at the low end of the supply voltage range. This high-impedance termination results in vulnerability to high-energy or high-frequency noise generated by bipolar or other non-CMOS components. Such noise must be held to manageable levels on both CMOS power and signal lines.
- Where CMOS must interface between logic frames or between different equipments, ground differences must be controlled in order to maintain operation within absolute maximum ratings.
Capacitance on a CMOS input or output will result in a forward-bias condition when power is turned off. This capacitance must discharge through forward-biased input or output to substrate junctions as the bus voltage collapses. Excessive capacitance (thousands of pF) should be avoided as discharging the stored energy may generate excessive current densities during power-down.

Where forward-biasing is inevitable, current limiting should be provided. Current should not be permitted to exceed 1mA on any package pin excluding supply pins.

All CMOS is susceptible to damage due to electrical overstress. It is the user's responsibility to follow a few simple rules in order to minimize device losses.

He should first select a source for the CMOS device that employs an effective input protection scheme. This will allow a greater margin of safety at all levels of device handling since the devices will not be quite so prone to static charge damage. Next, he should apply a sound set of handling and design rules. At minimum, this will eliminate electrical stressing or hold it to manageable levels.

With an effective on-chip protection scheme, good handling procedures and sound design, users should not lose any CMOS devices to electrical overstress.

Section 2. Reliability Screening Programs

Reliability Screening Programs

Facility Qualification

Harris is closely attuned to the requirements of military quality and reliability manufacturing programs. Our facilities and its quality plan is well accepted at all major companies. In addition, we have JAN qualification in the Bipolar Memory area and have JAN qualifications in process on CMOS Memory and Linear products.

MIL-STD-883 Class B (Dash 8)

As a special service to users of high rel products Harris makes instantly available high reliability on many of our product lines. Simply by adding its postscript -8 to appropriate Harris part numbers “off the shelf” delivery can be obtained of products screened to MIL-STD-883 Method 5004 Class B.
Hi-Rel Program

To meet our commitment to CMOS growth, Harris has introduced the Hi-Rel Dash 8 program. This program is designed to meet the needs of the customer seeking enhanced quality and reliability by additional screening steps.

This program is designed for:

- Customers using a current reliability add-on program.
- For the individual seeking a trade-off between additional cost and improved reliability and quality through screening — Harris gives a broad selection from Class B flow to burn-in only.

The Harris Hi-Rel Program is a comprehensive program aimed at serving the various needs of many customers. With the increasing need for improved IC systems mean time to failure performance, the Hi-Rel program assures high quality and reliability of CMOS circuits. Harris CMOS devices have been produced for over 6 years in modern state of the art manufacturing facilities. Our implemented second and third generation mask designs with the experience of well-controlled processes, results in standard products with built-in reliability. Coupling Harris CMOS with a Hi-Rel program will result in an enhanced combination for quality and reliability.

User Benefits

- Eliminates user screening programs
- Provides uncomplicated incoming inspection
- Reduces infant mortality and board rework
- Reduces field failures and unnecessary maintenance costs

Quality

In theory, parts tested 100 percent should upon receipt at the user's site be 100 percent good. Due to mass production there may exist a small percentage of parts which escape 100 percent tests. The AQL or LTPD outgoing sampling plans at Harris have been very successful in stopping the DOA's (Dead on Arrival). For the user with complex systems using large quantities of products, a quality enhancement can be tailored into your specific Hi-Rel program by choosing tightened sampling plans. The tightened quality test plan ensures close maintenance of the improved quality level through careful product segregation and retesting.

Reliability

Experience and perfected process controls have built reliability into a standard Harris CMOS product. Reliability cannot be tested into a part. Quality level may be improved by retesting and tighter sampling plans. However, reliability is improved by proper design and observance of sound ground rules, controlled processes and finally by stress testing to confirm claimed reliability performance. The Hi-Rel program offers a varied mix of stress tests to compress time and weed out devices subject to infant mortality. The equivalent early life failures are removed by the various screens such as temperature cycling, stabilization bake, burn-in and high temperature functional testing. Some or all of these stress tests will remove early failures and thus improve overall system reliability.
**INTRODUCTION**

**Statement of Scope**

This section establishes the detail requirements for Harris’ circuits screened and tested under the Product Assurance Program.

The Harris DASH 8 Devices pass the screening requirements of the latest issue of MIL-STD-883, Method 5004, Class B, and the requirements as specified in this document. Included in this section are the quality standards and screening methods for commercial parts which must perform reliably in the field.

**Applicable Documents**

The following Military documents form a part of this section to the extent referenced herein and provide the foundation for Harris Products Assurance Program.

- MIL-M-38510  "General Specification for Microcircuits"
- MIL-Q-9858A  "Quality Program Requirements"
- MIL-STD-883  "Test Methods and Procedures for Microelectronics"
- NASA Publication 200-3  "Inspection System Provisions"

Harris maintains a Product Assurance Program (PAP) using MIL-M-38510 as a guide. Harris Product Assurance Program assures compliance with the requirements and quality standards of control drawings and the requirements of this specification.

The DASH 8 Program will also be found useful by those Harris customers who must generate their own procurement specifications. Use of the enclosed Harris Standard Test Tables, Test Parameters, and Burn-In Circuits will aid in reducing specification negotiation time.

**PRODUCT ASSURANCE AT HARRIS**

Our Product Assurance Department strives to assure that the quality and reliability of products shipped to customers is of a high quality level and consistent with customer requirements. During product processing, there are several independent visual and electrical checks performed by Quality Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met. The system and procedures used and implemented are in accordance with MIL-M-38510, MIL-Q-9858A, MIL-STD-883A, MIL-C-45662 and MIL-I-45208.

The Harris Semiconductor Reliability and Quality Manual which is available upon request, describes the total function and policies of the organization to assure product reliability and quality.
HARRIS SEMICONDUCTOR DASH 8 PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

<table>
<thead>
<tr>
<th>SCREEN</th>
<th>MIL-STD-883 METHOD/COND.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Internal Visual</td>
<td>2010 Cond. B.</td>
</tr>
<tr>
<td>2. Stabilization Bake</td>
<td>1008 Cond. C (24 hrs. minimum)</td>
</tr>
<tr>
<td>3. Temperature Cycling</td>
<td>1010 Cond. C</td>
</tr>
<tr>
<td>4. Constant Acceleration</td>
<td>2001 Cond. E; Y1 plane</td>
</tr>
<tr>
<td>5. Seal: (A) Fine (B) Gross</td>
<td>40 Pin Cerdip, Cond. C; Y1 plane</td>
</tr>
<tr>
<td>6. Initial Electrical</td>
<td>1014 Cond. A or B</td>
</tr>
<tr>
<td>7. Burn-In Test</td>
<td>1014 Cond. C2</td>
</tr>
<tr>
<td>8. Final Electrical 100% go-no-go</td>
<td>Harris Specifications</td>
</tr>
<tr>
<td>9. External Visual</td>
<td>Tested at Worst Case Operating Conditions</td>
</tr>
<tr>
<td>10. Lot Acceptance</td>
<td>2009 Sample Inspection</td>
</tr>
</tbody>
</table>

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the HX-XXXX-8 and EIA date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

Additional Requirements: Attributes data will be supplied on Group A Lot Acceptance upon request.

Generic data from Harris' Reliability Add-On Program is available upon request. The objective of Harris Reliability Add-On Program is to provide a continuous life and environmental monitor for all products families in manufacturing. This program provides life test performance results to fulfill reliability data requirements and to verify package integrity. The Reliability Add-On Program is supplemental to customer funded Lot Qualification.

For customers desiring Lot Qualification, Harris Semiconductor will perform Group A, B, C and D inspections to MIL-STD-883, Method 5005 as defined herein for an additional charge.
# STANDARD PRODUCTS SCREENING AND INSPECTION PROCEDURE

<table>
<thead>
<tr>
<th>OPER. SEQ.</th>
<th>OPER. DESCRIPTION</th>
<th>PRODUCT CATEGORIES</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MIL (M)</td>
</tr>
<tr>
<td></td>
<td>Incoming Material Silicon and Chemical Procurement.</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>O.C. Incoming Inspection. Materials are Inspected for Conformance to Specified Requirements.</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Manufacturing Wafer Fabrication</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>QC • DIH₂O &amp; Gas Monitor • SEM Process Control • Wafer Process Control</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Manufacturing, Wafer Electrical Probe (100%)</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Manufacturing, Wafer Scribe, Break (100%)</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Manufacturing Dice Screen (100%)</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>QA Dice Inspection Control</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Preform Procurement</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Package Procurement</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Leadframe Procurement</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Epoxy Compound Procurement</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Q.C. Preform Inspection</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Q.C. Package Inspection</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Q.C. Leadframe Inspection</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Manufacturing Package Clean</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>Manufacturing Die Mounting</td>
<td>X</td>
</tr>
<tr>
<td>Process</td>
<td>M</td>
<td>C</td>
</tr>
<tr>
<td>----------------------------------------------</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>QA Die Mount Control (continuous sampling)</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>• Visual Die Inspection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bond Wire Procurement</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Q.C. Wire Inspection (receiving)</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Manufacturing Wire Bonding</td>
<td>X</td>
<td>Al</td>
</tr>
<tr>
<td>QA Bond Control (continuous sampling)</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>• Visual Die &amp; Bond Inspection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>• Wire and Pull Test</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Manufacturing Pre-Seal Screen (100%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QA Pre-Seal Inspection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lot Acceptance</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Preseal Bake Per MS-883, Method 1008, Cond. C</td>
<td>8 hr.</td>
<td>4 hr.</td>
</tr>
<tr>
<td>Package Lid Procurement</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Package Lid Inspection</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Package Lid Clean</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Package Seal/Encapsulation</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
Stabilization Bake
MS-883, Method 1008, Cond. C.
24 hr. 8 hr. 8 hr.

Temperature Cycle, MS-883,
Method 1010, Cond. C.

Centrifuge, MS-883, Method 1010,
(Y1) Plane 30 KG's min.
40 Pin Cerdip Package 5H
15 KG's min.
Fine Leak, MS-883, Method 1014
100% X N/A

Gross Leak, MS-883, Method 1014
Condition C2
100% X N/A

Frame Removal & Loading Units
In Carriers/Sticks
X X X

Final QA Lot Inspection, MS-883
Method 1014
• Fine & Gross Leak
• Visual/Mechanical Inspection

Group A Initial Tests 1.

Brand Device Type/Date Code
Serialize, If Applicable
X N/A N/A

Burn-In (100%), MS-883,
Method 1015
Classes A/B
Products N/A N/A

Group A Final Test (100%)
(Worst Case Oper. Cond.)
X N/A N/A

QA Acceptance Elec. Testing
• Visual/Mechanical Method
2009 Lot Sampling
X X X

Brand Device Type/Date Code
N/A X X

Controlled Inventory
X X X
HARRIS COMMERCIAL GRADE PRODUCTS

This product is processed on the same wafer fabrication lines, to the same thorough specification and rigid controls as HI-Rel parts. At wafer electrical probe the product may be categorized for electrical performance, such as temperature range of operation or maximum output (see specific product data sheet for grading details) by utilizing multiple colored inks. Defective die are inked with red ink, but, for example, die meeting the commercial temperature range electrical specifications may be inked with green ink.

The die are then visually inspected and sorted after die separation to a modified Class B visual criteria. They are then assembled in packages on a controlled assembly line. The ink used to categorize product performance, such as the green ink, might not be removed from the commercial grade die. This ink has been chemically characterized as inert and reliability verification confirms there is no effect on performance or operating life of the parts.

Harris invites any interested customer to review our assembly flow and facilities for information, quality survey, or certification.
### TABLE I – GROUP A ELECTRICAL TESTS

<table>
<thead>
<tr>
<th>SUBGROUP&lt;sup&gt;2&lt;/sup&gt;</th>
<th>CLASSES S &amp; B LTPD</th>
<th>CLASS C LTPD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Subgroup 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Static Tests at 25°C</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Subgroup 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Static Tests at Max. Rated Operating Temperature</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>Subgroup 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Static Tests at Min. Rated Operating Temperature</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>Subgroup 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Functional Tests at 25°C</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Subgroup 8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Functional Tests at Max. and Min. Rated Operating Temperatures</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>Subgroup 9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Tests at 25°C</td>
<td>7</td>
<td>10</td>
</tr>
<tr>
<td>Subgroup 10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Tests at Max. Rated Operating Temperature</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>Subgroup 11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Tests at Min. Rated Operating Temperature</td>
<td>10</td>
<td>15</td>
</tr>
</tbody>
</table>

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2. A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100% inspection shall be allowed (see 30.2.5 of Appendix B of MIL-M-38510).
**TABLE II — GROUP B TESTS (LOT RELATED)**

<table>
<thead>
<tr>
<th>TEST</th>
<th>METHOD</th>
<th>CONDITION</th>
<th>LTPD*</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Subgroup 1</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Physical Dimensions</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2016</td>
<td></td>
<td>2 Devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(No Failures)</td>
</tr>
<tr>
<td><strong>Subgroup 2</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>a. Resistance to Solvents</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2015</td>
<td></td>
<td>3 Devices</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(No Failures)</td>
</tr>
<tr>
<td>b. Internal Visual and Mechanical</td>
<td></td>
<td>Failure Criteria from Design and Construction Requirements of Applicable</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Procurement Document</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2014</td>
<td></td>
<td>1 Device</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(No Failures)</td>
</tr>
<tr>
<td>c. Bond Strength 2.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(1) Thermocompression</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(2) Ultrasonic or Wedge</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(3) Beam Lead</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2011</td>
<td></td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>(1)</td>
<td>Test Condition C or D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(2)</td>
<td>Test Condition C or D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(3)</td>
<td>Test Condition H</td>
<td></td>
</tr>
<tr>
<td><strong>Subgroup 3</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Solderability 3.</td>
<td>2003</td>
<td>Soldering Temperature of 260 ±10°C</td>
<td>15</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.

2. Test samples for bond strength may, at the manufacturer’s option unless otherwise specified be randomly selected immediately following internal visual (precap) inspection specified in method 5004, prior to sealing.

3. All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

4. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note – Table 1*
### TABLE III – GROUP C (DIE-RELATED TESTS)

<table>
<thead>
<tr>
<th>TEST</th>
<th>METHOD</th>
<th>CONDITION</th>
<th>LTPD*</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Subgroup 1</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Life Test</td>
<td>1005</td>
<td>Test Condition to be specified (1000 Hrs)</td>
<td>5</td>
</tr>
<tr>
<td>End Point Electrical Parameters</td>
<td></td>
<td>Table I – Subgroup 1</td>
<td></td>
</tr>
<tr>
<td><strong>Subgroup 2</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Cycling</td>
<td>1010</td>
<td>Test Condition C</td>
<td>15</td>
</tr>
<tr>
<td>Constant Acceleration</td>
<td>2001</td>
<td>Test Condition E, 40 Pin Cerdip, Cond. C Y1 Axis</td>
<td></td>
</tr>
<tr>
<td>Seal</td>
<td></td>
<td>As Applicable</td>
<td></td>
</tr>
<tr>
<td>(a) Fine</td>
<td>1014</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(b) Gross 2.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Visual Examination</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>End Point Electrical Parameters</td>
<td></td>
<td>Table I – Subgroup 1</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

1. Visual examination shall be in accordance with method 1010.
2. When fluorocarbon gross leak testing is utilized, test condition C2 shall apply as minimum.
3. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note – Table 1 *
### TABLE IV – GROUP D (PACKAGE RELATED TESTS)

<table>
<thead>
<tr>
<th>TEST</th>
<th>METHOD</th>
<th>CONDITION</th>
<th>LTPD*</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Subgroup 1</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Physical Dimensions</td>
<td>2016</td>
<td></td>
<td>15</td>
</tr>
<tr>
<td><strong>Subgroup 2</strong> 4.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lead Integrity</td>
<td>2004</td>
<td>Test Condition B2 (Lead Fatigue)</td>
<td>15</td>
</tr>
<tr>
<td>Seal</td>
<td>1014</td>
<td>As Applicable</td>
<td></td>
</tr>
<tr>
<td>(a) Fine</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(b) Gross 6.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Subgroup 3</strong> 1.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Shock</td>
<td>1011</td>
<td>Test Condition B as a Minimum, 15 Cycles Minimum.</td>
<td>15</td>
</tr>
<tr>
<td>Temperature Cycling</td>
<td>1010</td>
<td>Test Condition C, 10 Cycles Minimum</td>
<td></td>
</tr>
<tr>
<td>Moisture Resistance</td>
<td>1004</td>
<td>Omit Initial/Conditioning and Vibration</td>
<td></td>
</tr>
<tr>
<td>Seal</td>
<td>1014</td>
<td>As Applicable</td>
<td></td>
</tr>
<tr>
<td>(a) Fine</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(b) Gross 6.</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Visual Examination</td>
<td>2.</td>
<td>Table I — Subgroup 1</td>
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<td>End Point Electrical Parameters</td>
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<td><strong>Subgroup 4</strong> 1.</td>
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<td>Mechanical Shock</td>
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<td>Vibration Variable Frequency</td>
<td>2007</td>
<td>Test Condition A</td>
<td></td>
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<td>Constant Acceleration</td>
<td>2001</td>
<td>Test Condition E, 40 Pin Cerdip, Cond. C</td>
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<td>Seal</td>
<td>1014</td>
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<td>(a) Fine</td>
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<td>(b) Gross 6.</td>
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<tr>
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<td>Table I — Subgroup 1</td>
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<td>Salt Atmosphere</td>
<td>1009</td>
<td>Test Condition A</td>
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<tr>
<td>Visual Examination</td>
<td>5.</td>
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</tr>
</tbody>
</table>

**NOTES:**

1. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
2. Visual examination shall be in accordance with method 1010 or 1011 at a magnification of 5X to 10X.
3. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
4. Electrical reject devices from that same inspection lot may be used for samples.
5. Visual examination shall be in accordance with paragraph 3.3.1 for method 1009.
6. When fluorocarbon gross leak testing is utilized, test condition C2 shall apply as minimum.
7. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note – Table 1 *
### Section 3. Burn-In Circuits

#### Burn-In Circuit Index

<table>
<thead>
<tr>
<th>MICROPROCESSOR FAMILY</th>
<th>DRAWING NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>HM-6100 CMOS 12 Bit Microprocessor (CPU)</td>
<td>1</td>
</tr>
<tr>
<td>HD-6101 CMOS Parallel Interface Element (PIE)</td>
<td>2</td>
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<tr>
<td>HD-6102 (Advance) Memory Extension/DMA/Interval Timer/Controller (MEDIC)</td>
<td></td>
</tr>
<tr>
<td>HD-6103 (Advance) CMOS Parallel Input/Output Port (PIO)</td>
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<thead>
<tr>
<th>MEMORY FAMILY</th>
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<tr>
<td>HM-6312 CMOS ROM 1024 Word x 12 Bit</td>
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<tr>
<td>HM-6512 64 x 12 CMOS RAM</td>
<td>4</td>
</tr>
<tr>
<td>HM-6561 256 x 4 CMOS RAM</td>
<td>5</td>
</tr>
<tr>
<td>HM-6518 1024 x 1 CMOS RAM</td>
<td>6</td>
</tr>
<tr>
<td>HM-6533 1024 x 4 CMOS RAM</td>
<td>7</td>
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<tr>
<td>HM-6543 4096 x 1 CMOS RAM</td>
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<tr>
<th>INTERFACE FAMILY</th>
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<tr>
<td>HD-4702 CMOS Programmable Bit Rate Generator</td>
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<tr>
<td>HD-6402 CMOS/LSI Universal Asynchronous Receiver Transmitter (UART)</td>
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</tr>
<tr>
<td>HD-6405 CMOS Programmable Bit Rate Generator</td>
<td>9</td>
</tr>
<tr>
<td>HD-6408 CMOS Asynchronous Serial Manchester Adapter (ASMA)</td>
<td>11</td>
</tr>
<tr>
<td>HD-6431 CMOS Hex Latched Bus Driver</td>
<td>12</td>
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<tr>
<td>HD-6432 CMOS Hex Bi-directional Bus Driver</td>
<td>13</td>
</tr>
<tr>
<td>HD-6433 CMOS Quad Bus Transceiver</td>
<td>14</td>
</tr>
<tr>
<td>HD-6434 (Advance) CMOS Octal Resettable Latched Bus Driver</td>
<td>15</td>
</tr>
<tr>
<td>HD-6435 (Advance) CMOS Hex Resettable Latched Bus Driver</td>
<td>16</td>
</tr>
<tr>
<td>HD-6436 (Advance) CMOS Octal Bus Buffer Driver</td>
<td>17</td>
</tr>
<tr>
<td>HD-6440 CMOS Latched 3 to 8 Line Decoder Driver</td>
<td>18</td>
</tr>
<tr>
<td>HD-6495 CMOS Hex Bus Driver</td>
<td>19</td>
</tr>
</tbody>
</table>
NOTES: Use standard CMOS DRIVER with fO = 1MHz. Pins 11 to 12 should be the closest 4 frequencies on the 4040 counter.

12 - Pin 1
11 - Pin 15
10 - Pin 14
9 - Pin 12

CLOCK IN
10 = 1MHz

All load resistors on the HD-6408 are 1.8KΩ 20% 1/4 watt.
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<thead>
<tr>
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<th>7–2</th>
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</thead>
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<td>Package Selection Guide</td>
<td>7–3</td>
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<tr>
<td>Package Dimensions</td>
<td>7–4</td>
</tr>
</tbody>
</table>
Component Ordering Information

<table>
<thead>
<tr>
<th>PREFIX:</th>
<th>H - Harris</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAMILY:</td>
<td>A - Analog, C - Communications, D - Digital, I - Interface, M - Memory</td>
</tr>
<tr>
<td>PACKAGE CODE:</td>
<td>0 - Chip Form, 1 - Ceramic, 3 - Epoxy, 4 - Leadless Carrier, 9 - Flatpack</td>
</tr>
<tr>
<td>PART NUMBER:</td>
<td>OXXX - Diode Matrices, 61XX - Microprocessor, 63XX - CMOS ROMs, 64XX - CMOS Interface, 65XX - CMOS RAMs, 66XX - CMOS PROMs, 76XX - Bipolar PROMs</td>
</tr>
<tr>
<td>TEMPERATURE:</td>
<td>2 - -55°C to +125°C, 5 - 0°C to +75°C, 6 - 100% 250°C Probe, 8 - Dash 8 Program, 9 - -40°C to +85°C</td>
</tr>
<tr>
<td>VERSION:</td>
<td>A - 10.0V Nominal, C - Relax 5.0V Nominal, Blank - 5.0V Nominal</td>
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System Ordering Information

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<thead>
<tr>
<th>PREFIX:</th>
<th>H - Harris</th>
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<tr>
<td>FAMILY:</td>
<td>B - Board &amp; Systems, Z - Documentation</td>
</tr>
<tr>
<td>PACKAGE CODE:</td>
<td>0 - Systems</td>
</tr>
<tr>
<td>PART NUMBER:</td>
<td>61XXX - Systems</td>
</tr>
<tr>
<td>OPTION:</td>
<td>61000-1 - Basic system with 256 words memory, 61000-4 - Basic system with 1024 words memory &amp; parallel I/O port, 61000-5 - Basic system with 256 words memory &amp; parallel I/O port in kit form, 61001-1 - 4096 word CMOS memory, 61001-2 - 2048 word CMOS memory</td>
</tr>
</tbody>
</table>

HARRIS DASH 8 PROGRAM

As a service to users of High Rel products, Harris makes readily available via the high reliability DASH 8 program many products from our product lines. Parts screened to MIL-STD-883 Method 5004 Class B are simply branded with the postscript "-8" to the appropriate Harris part numbers, in effect, offering "off the shelf" delivery. For details concerning this special Harris program for High Rel users, see the Dash 8 section of this Data Book.
SPECIAL ORDERS

For best availability and price, it is urged that standard “Product Code” devices be specified, which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard “Dash 8” screening described in the Data Book. Harris application engineers may be consulted for advice about suitability of a part for a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Since many electrical parameters may be economically assured through design analysis, characterization, or correlation with other parameters should be labeled “Vendor will guarantee, but not necessarily test”.

Harris reserves the right to decline to quote or to request modification to special screening requirements.

Package Selection Guide

<table>
<thead>
<tr>
<th>PRODUCT</th>
<th>CERDIP</th>
<th>EPOXY</th>
<th>LEADLESS</th>
<th>FLATPACK †</th>
<th>CERPACK †</th>
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<tr>
<td>Microprocessor Family</td>
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<tr>
<td>HM-6100</td>
<td>4J (5H)**</td>
<td>3H</td>
<td>LG</td>
<td>9X</td>
<td>8P</td>
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<tr>
<td>HD-6101</td>
<td>4J (5H)**</td>
<td>3J</td>
<td>LG</td>
<td>9X</td>
<td>8P</td>
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<tr>
<td>HD-6102 (Advance)</td>
<td>4J (5H)**</td>
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<td>HD-6103 (Advance)</td>
<td>4J (5H)**</td>
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<td>8C</td>
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<td>9B</td>
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</table>

* These package numbers to be used in product ordering. Other numbers shown in Selection Guide and drawings are internal numbers.

** Harris is making a transition from the 4J to the 5H package. Check with your local rep before placing an order to determine the current package type.

† Harris is making a transition from flatpacks to cer-packs. Check with your local rep before placing an order to determine the current package type.

NOTE FOR PACKAGE DRAWINGS ON FOLLOWING PAGES:
1. All dimensions in inches; millimeters are shown in parenthesis.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.
3. Internal package codes are shown in black squares.
Package Dimensions

3D
18 LEAD D.I.P. EPOXY

3E
22 LEAD D.I.P. EPOXY

3F
24 LEAD D.I.P. EPOXY

3H
40 LEAD D.I.P. EPOXY

3L
16 LEAD D.I.P. EPOXY

3N
20 LEAD D.I.P. EPOXY

4G
18 LEAD CERAMIC D.I.P.

4J
40 LEAD SIDE BRAZED D.I.P.
Dice Information

Dice Ordering Information  8–2
Dice Geometry Index  8–3
Dice Geometries & Dimensions  8–4
Dice Ordering Information

GENERAL INFORMATION

Harris Microprocessor Products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested at 25°C to the data sheet limits for the commercial device and are 100% visually inspected to MIL-STD-883, Method 2010, condition B criteria. Packaging for shipment consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

The hybrid industry has rapidly become more diversified and stringent in its requirements for integrated circuits. To meet these demands Harris has several options additional to standard chip processing available upon request at extra cost. For more information consult your nearest Harris Sales Office.

CHIP ORDERING INFORMATION

Standard and special chip sales are direct factory order only. The minimum order on all sales is $250.00 per line item. Contact the local Harris Sales Office for pricing and delivery on special chip requirements.

MECHANICAL INFORMATION

Dimensions: All chip dimensions nominal with a tolerance of ± .003". Maximum chip thickness is .012".
Bonding pads: Minimum bonding pad size is .004" x .004" unless otherwise specified.

PRODUCT CODE EXAMPLE

H M O 6100 A 6

HARRIS
FAMILY:
D: Digital
M: Memory
PACKAGE CODE:
0: Chip form

PART NUMBER

TEMPERATURE:
*2: -55°C to +125°C
6: 100% 25°C probe

VERSION:
A: 10.0V Nominal
C or BLANK: 5.0V Nominal, lowest electrical grade

* Contact Harris for Availability

NOTE: All Harris Digital Microprocessor Products have biased substrates. Persons wishing to utilize products in dice form should contact the Harris factory for specific product information regarding proper connection of the substrate.
# Dice Geometry Index

<table>
<thead>
<tr>
<th>Product</th>
<th>Description</th>
<th>Drawing No.</th>
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</thead>
<tbody>
<tr>
<td><strong>MICROPROCESSOR FAMILY</strong></td>
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</tr>
<tr>
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<td><strong>INTERFACE FAMILY</strong></td>
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<tr>
<td>HD-4702</td>
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<td>HD-6495</td>
<td>CMOS Hex Bus Driver</td>
<td>13</td>
</tr>
</tbody>
</table>
Harris Sales Locations

OEM Sales

NORTHEASTERN REGION
Suite 301
177 Worcester Street
Wellesley Hills, MA 02181
(617) 237-5430
535 Broadhollow Road
Melville, L.I., NY 11747
(516) 249-4500

SOUTHEASTERN REGION
Suite 115
2020 W. McNab Road
Ft. Lauderdale, FL 33309
(305) 971-3200
Suite 325
650 Swedesford Road
Wayne, PA 19087
(215) 687-6680

CENTRAL REGION
16001 Dallas Parkway
Mail Stop 47
Dallas, TX 75240
(214) 386-2090
Suite 206
5250 Far Hills Avenue
Kettering, OH 45429
(513) 433-5770
Suite 508
2355 S. Arlington Heights Road
Arlington Heights, IL 60005
(312) 437-4712

WESTERN REGION
Suite 227
21243 Ventura Boulevard
Woodland Hills, CA 91364
(213) 992-0686
2016 Quail Street
Newport Beach, CA 92660
(714) 540-2176
Suite 300
625 Ellis Street
Mountain View, CA 94043
(415) 964-6443

International Sales

Europe

OEM SALES OFFICES

ENGLAND
Harris Systems Ltd.
Harris Semiconductor Div.
P.O. Box 27, 145 Farnham Rd.
Slough SL1 4XD
Tel: (Slough) 34666
TWX: 848174 HARRIS G

BELGIUM
Harris Semiconductor Inc.
53 Blvd de Waterloo Bte 5
B-1000 Brussels
Tel: 02-511-08-24
TWX: 26382 HARRIS B

FRANCE
Harris S. A.
Harris Semiconductor
4 Avenue Charles de Gaulle
F-78150 Le Chesnay
Tel: 954-90-77
TWX: 842 696 514 F HARRISP

WEST GERMANY
Harris GmbH
Harris Semiconductor Div.
Einsteinstrasse 127
D-8 Munich 80
Tel: 089-47-30-47
TWX: 524126 HARMU D

EUROPEAN DISTRIBUTORS

AUSTRIA
Kontron GmbH
Amelisgasse 49
A-1140 Vienna
Tel: 945646
TWX: 11699 KONIN A

BELGIUM
Betea S. A.
775 Che de Louvain
B-1140 Brussels
Tel: 02-7368050
TWX: 23188 BETEA B

DENMARK
Ditz Schweitzer A. S.
Vallensbaekvej 41
DK-2600 Glostrup
Tel: 02-453044
TWX: 33257 SCHWEI DK

FINLAND
Finn Metric OY
Ahertajantie 6 D/PL 35
SF-02101 Espoo 10
Tel: 460 844
TWX: 122018 TRIC SF

FRANCE
Almex S. A.
48, rue de l'Aubepine
F-92160 Antony
Tel: 666-21-12
TWX: 250067 ALMEX

A 2 M
18 Avenue Dutartre
F-78150 Le Chesnay
Tel: 955-32-49
TWX: 698 376 AMM

Spetelec
Tour Europa-Belle Epine
Cidex A III
F-94532 Rungis
Tel: 686 5665
TWX: 25.801 THAI

GERMANY
Alfred Neye-Enatechnik GmbH
Schillerstrasse 14
2086 Quickborn b. Hamburg
Tel: 041 06 612 1
TWX: 02-13 590 ENA D

Kontron Elektronik GmbH
Breslauer Str. 2
D-8057 Eching b. Munich
Tel: 89 31 90 11
TWX: 0522122 KONEL D
EUROPEAN DISTRIBUTORS (Germany continued)

Jermyn GmbH
Schulstrasse 36
D-6277 Camberg-Würges
Tel: (06434) 6005
TWX: 484426 JERM D

ITALY

Erie Elettronica SpA
Via Melchiorre Gioia 66
I-20125 Milano
Tel: (2)6884833/4/5
TWX: 36385 ERIEMIL

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