BURROUGHS
D84
MODULAR INTEGRATED CIRCUIT
MILITARY COMPUTER

Burroughs Corporation
BURROUGHS
D84
MODULAR INTEGRATED CIRCUIT MILITARY COMPUTER

CHARTS 1 THROUGH 11 — INTRODUCTION
CHARTS 12 THROUGH 27 — LOGIC/SYSTEM
CHARTS 28 THROUGH 37 — CIRCUITS
CHARTS 38 THROUGH 51 — PACKAGING
CHARTS 52 THROUGH 54 — SUMMARY

Burroughs Corporation
1. FUNCTIONAL MODULARITY - MATRIX ORGANIZATION

D825 - 1962
D830 - 1964
B8500-1966

2. ADVANCED MICROCIRCUIT TECHNIQUES*, AND

3. ADVANCED MAULER COMPUTER DESIGN**

* FEB. '64 COMPLETION OF 12-BIT ARITHMETIC UNIT (700 I.C.'s) — LIFE-TEST CONTINUING.

** TO IMPROVE T.E.C. (REDUCE IN SIZE, INCREASE MTBF)
COMBINED TO PRODUCE D84*

FEATURING PHYSICALLY INDEPENDENT FUNCTIONAL MODULES
ALL LOGIC IMPLEMENTED WITH MONOLITHIC INTEGRATED CIRCUITS

FOR FLEXIBILITY IN SYSTEMS CONFIGURATIONS
GROWTH POTENTIAL BUILT-IN
COMPACT
RELIABILITY
LIGHT-WEIGHT
LOW POWER CONSUMPTION

PROTOTYPE (OPERATIONAL JANUARY '65) DIFFERS FROM PRODUCTION D84
(1) PACKAGING MORE COMPACT—100% FLATPACK UTILIZATION/LOGISTICAL DISADVANTAGE, AND
(2) INSTRUCTION REPERTOIRE—35 BASIC COMMANDS VS. 47

* NOV. '63 START-UP.
OVER 100 TYPES -- ALL FLATPACKS USED: LINE MAINTENANCE AT FUNCTIONAL MODULE LEVEL
D84 C. N. M. -"2-D"

35 MAX. TYPES (ONLY 23 IN LOGIC*) : AVERAGE FLATPACK UTILIZATION 10 TO 11 PER CNM: LINE. MAINTENANCE AT CNM (THROWAWAY) LEVEL—MADE PRACTICAL VIA DIAGNOSTICS PROGRAM

* i.e. EXCLUDING MEMORY AND SPECIAL I/O CIRCUITS
MAJOR ADVANTAGES

1. LOW COST

   - DEVELOPMENT COMPLETE
   - ONE TIME CHARGES RESTRICTED TO DESIGN OF SPECIAL INTERFACES IN THE I/O MODULE.

2. MODULAR EXPANSIBILITY THROUGH TO MULTIPROCESSING FOR MORE THROUGHPUT AND/OR GRACEFUL DEGRADATION.

3. MULTIPLE INDEXING

   - MULTI-LEVEL INDIRECT ADDRESSING
   - VERSATILE INSTRUCTION REPERTOIRE
   - LEADING TO REDUCED MEMORY REQUIREMENTS AND/OR REDUCED RUNNING TIME.
MAJOR ADVANTAGES CONTINUED

4. AGGRESSIVE INTERRUPT SYSTEM

- PROGRAMMABLE PRIORITIES
- INTERRUPTS MAY BE IGNORED OR STORED FOR DEFERRED ACTION - 24 MAX. INTERRUPTS

5. FLEXIBILITY OF I/O

- CHANNEL TYPE AND NUMBER TAILORED TO APPLICATION
- PACKAGING FLEXIBILITY TO MAINTAIN LOWEST PRACTICAL SIZE FOR SPECIFIED I/O DESIGN - 3 STANDARD PACKAGES

6. EXTENDED PRODUCT LIFE

- MODULAR GROWTH - IN MEMORY, I/O, & CENTRAL DATA ProcessORS(MULTI-PROCESSING)
- HIGHER SPEED CIRCUITS FOR SYSTEM SPEED-UP WHEN USED WITH THIN-FILM MEMORIES (8:1 BY LAST QUARTER '67 DELIVERIES) — PROGRAM COMPATIBLE WITH PRESENT SYSTEM.
MAJOR ADVANTAGES CONTINUED

7. MAINTENANCE

- NO PREVENTIVE MAINTENANCE
- EMERGENCY MAINTENANCE PHILOSOPHY SELECTED BY CUSTOMER

1. ON-LINE, WHILE SYSTEM IS OPERATIVE (MULTI-PROCESSING) - NO DOWNTIME

2. AT FUNCTIONAL MODULE LEVEL - <5 MIN. DOWNTIME

3. AT CIRCUIT NETWORK MODULE LEVEL - 30 MIN. DOWNTIME

4. AT FLATPACK LEVEL
D84 - AVERAGE INSTRUCTION EXECUTE TIME

1. "COMMAND AND CONTROL MIX" — COMMUNICATIONS OF THE ACM — MAY '64
   A) WITH 4μS CYCLE TIME MEMORY - 10μS
   B) WITH 3μS CYCLE TIME MEMORY - 8μS
   VS.  360/40 - 14μS
        360/50 - 5μS

2. "GIBSON MIX" — SCIENTIFIC CALCULATIONS
   A) WITH 4μS CYCLE TIME MEMORY - 19μS
   B) WITH 3μS CYCLE TIME MEMORY - 15μS
   VS.  360/40 - 30μS
        360/50 - 7½μS
SOFTWARE - INITIAL DELIVERIES
(LATE '65 THRU 1st. HALF OF '66)

1. ASSEMBLER PROGRAM - FORTRAN IV FOR 7044 AND 7094
   - SYMBOLIC MNEMONICS SPECIFY OPERATIONS
   - SYMBOLIC TAGS SPECIFY MEMORY REFERENCES
   - OBJECT PROGRAM PRODUCED (CARD DECK) FOR D84
   - PROGRAM DECK PRODUCED FOR INPUT TO SIMULATOR

2. SIMULATOR PROGRAM - FORTRAN IV FOR 7044 AND 7094
   - DEBUG OBJECT PROGRAM
   - MEASURES PROGRAM RUNNING TIME
SOFTWARE--INITIAL DELIVERIES (LATE '65 THRU 1st. HALF OF '66) CONTINUED

3. SUBROUTINES (FOR CALL-UP BY THE ASSEMBLER)

- SQUARE ROOT
- TRIGONOMETRIC FUNCTIONS
- INVERSE TRIGONOMETRIC FUNCTIONS
- POLYNOMIAL OF DEGREE \( n \)
- ASCII TO BINARY CONVERSION
- DOUBLE PRECISION MULTIPLY, DIVIDE

4. DIAGNOSTIC PROGRAM

- MINIMUM OPERATOR INTERVENTION
- LOCATES FAULT TO THROW-AWAY MODULES* - 9 MIN. MEAN TIME.

* TO A MAX. OF 5 CNM's, 90% OF THE TIME — TO AN ABSOLUTE MAX. OF 10 CNM's
# SUBROUTINES

<table>
<thead>
<tr>
<th>MNEMONIC</th>
<th>DESCRIPTION</th>
<th>REQUIRED STORAGE</th>
<th>EXECUTION TIME (MS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIN</td>
<td>SINGLE-PRECISION SIN</td>
<td>93</td>
<td>0.75</td>
</tr>
<tr>
<td>COS</td>
<td>SINGLE-PRECISION COS</td>
<td>93</td>
<td>0.75</td>
</tr>
<tr>
<td>INTAN</td>
<td>SINGLE-PRECISION TAN$^{-1}$</td>
<td>154</td>
<td>1.52</td>
</tr>
<tr>
<td>INSIN</td>
<td>SINGLE-PRECISION SIN$^{-1}$</td>
<td>123</td>
<td>2.35</td>
</tr>
<tr>
<td>INCOS</td>
<td>SINGLE-PRECISION CON$^{-1}$</td>
<td>123</td>
<td>2.35</td>
</tr>
<tr>
<td>SINCO</td>
<td>DOUBLE-PRECISION SIN OR COS</td>
<td>100</td>
<td>2.856</td>
</tr>
<tr>
<td>ARCTAN</td>
<td>DOUBLE-PRECISION TAN$^{-1}$</td>
<td>167</td>
<td>5.850</td>
</tr>
<tr>
<td>ASICO</td>
<td>DOUBLE-PRECISION SIN$^{-1}$ OR COS$^{-1}$</td>
<td>130</td>
<td>7.990</td>
</tr>
<tr>
<td>DPDIV</td>
<td>DOUBLE-PRECISION DIVIDE</td>
<td>37</td>
<td>0.416</td>
</tr>
<tr>
<td>DPMUL</td>
<td>DOUBLE-PRECISION MULTIPLY</td>
<td>33</td>
<td>0.248</td>
</tr>
<tr>
<td>SQRT</td>
<td>DOUBLE-PRECISION SQUARE-ROOT</td>
<td>52</td>
<td>1.762</td>
</tr>
<tr>
<td>POLNOM</td>
<td>DOUBLE-PRECISION POLYNOMIAL OF DEGREE n</td>
<td>47</td>
<td></td>
</tr>
</tbody>
</table>

where \( n = \text{number of terms less one} \)
BASIC D84M COMPUTER SYSTEM CONCEPT

CENTRAL DATA PROCESSOR MODULE

DATA
CONTROL
ADDRESS

MODULE INTERFACE CONTROL

DATA
ADDRESS AND TIMING

4096 WORD 25-BIT MEMORY MODULE

MEMORY IS EXPANDABLE TO EIGHT MODULES.

THERE ARE FOUR INDEPENDENT PROGRAM SELECTED TRANSFER PATHS WHICH MAY BE CONNECTED EXTERNALLY OR INTERNALLY

BASIC I/O MODULE

I/O INTERFACE CONTROL

TERMINAL DEVICES

THERE ARE FOUR INDEPENDENT PROGRAM SELECTED TRANSFER PATHS WHICH MAY BE CONNECTED EXTERNALLY OR INTERNALLY

1/0 INTERFACE CONTROL

DATA
CONTROL
ADDRESS

12.
MODULE FUNCTIONS

CENTRAL DATA PROCESSOR:
- ARITHMETIC UNIT
- INSTRUCTION EXECUTION
- INDEXING
- PROGRAM SEQUENCING
- MEMORY ADDRESSING

MODULE INTERFACE CONTROL:
- MEMORY ACCESS CONTROL
- DATA ROUTING
- PROGRAM INTERRUPTS
- START/STOP CONTROLS
- BOOTSTRAP CONTROLS
- CONSOLE INTERFACE

I/O INTERFACE CONTROL:
- TERMINAL DEVICE SELECTION
- DATA TRANSFER TIMING
- WORD BUFFER
- SPECIAL FUNCTIONS

MEMORY:
- PROGRAM STORE
- DATA STORE
- I/O BUFFER
FUNCTIONAL CHARACTERISTICS

OPERATION:
SYNCHRONOUS, PARALLEL

ARITHMETIC:
FRACTIONAL BINARY, FIXED POINT
SIGN PLUS 23 BITS MAGNITUDE

OPERATING SPEEDS:
ONE MEGACYCLE CLOCK
EXECUTION OF UP TO 333,000 INSTRUCTIONS/SEC.

COMMAND REPERTOIRE:
47 BASIC COMMANDS
OVER 300 USEFUL VARIATIONS

ADDRESSING:
SINGLE ADDRESS, DIRECT
MULTILEVEL INDIRECT
FUNCTIONAL CHARACTERISTICS (CONTINUED)

INDEXING:
INDEX REGISTERS IN MEMORY
NUMBER OF INDEX REGISTERS AND LOCATION PROGRAM DETERMINED

MEMORY:
MODULAR, 4096 WORD BASIC MODULE
EXPANDABLE TO 32768 WORDS (EIGHT MODULES)
ONE MICROSECOND ACCESS TIME
CYCLE TIME DETERMINED BY TYPE OF MEMORY

INPUT/OUTPUT:
MASKABLE INTERRUPTS
BUFFERED AND UNBUFFERED I/O CHANNELS
PROVISIONS FOR SPECIAL I/O FUNCTIONS
## EXECUTION TIMES

<table>
<thead>
<tr>
<th>COMMAND</th>
<th>4µsec.R/R</th>
<th>3µsec.R/R</th>
<th>2µsec.R/R</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADD</td>
<td>8</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>ADD LITERAL</td>
<td>4</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>ADD DOUBLE PRECISION</td>
<td>12</td>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>MULTIPLY</td>
<td>28</td>
<td>27</td>
<td>25</td>
</tr>
<tr>
<td>DIVIDE</td>
<td>51</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>STORE SINGLE WORD</td>
<td>8</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>STORE DOUBLE WORD</td>
<td>12</td>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>BRANCH</td>
<td>4</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>TEST (EQUAL, GREATER, LESS)</td>
<td>8</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>TEST (EQUAL, GREATER, LESS) LITERAL</td>
<td>4</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>TEST (EQUAL, GREATER, LESS) BLOCK OF BLOCK SIZE m</td>
<td>16+8(m-1)</td>
<td>12+7(m-1)</td>
<td>10+5(m-1)</td>
</tr>
</tbody>
</table>
TYPES OF STANDARD I/O

UNBUFFERED CHANNEL:
ADDRESSABLE TERMINAL DEVICES: 127
MAXIMUM DATA RATE:
4μ SEC MEMORY: 35 700 WORDS/SEC.
2μ SEC MEMORY: 50 000 WORDS/SEC

BUFFERED CHANNEL:
ADDRESSABLE TERMINAL DEVICES: 64
BUFFERED CHANNELS PER CDP: 16
MAXIMUM DATA RATE:
4μ SEC MEMORY: 250 000 WORDS/SEC.
2μ SEC MEMORY: 500 000 WORDS/SEC
TYPES OF STANDARD I/O CONTINUED

CIRCULATING BUFFERED CHANNEL:
MODIFIED BUFFERED CHANNEL FOR USE WITH DISPLAY

SINGLE WORD BUFFERED CHANNEL
ADDRESSABLE TERMINAL DEVICES 64
CHANNELS PER CDP 4
MAXIMUM DATA RATE:
4μ SEC MEMORY: 27500 WORDS / SEC.
2μ SEC MEMORY: 41 600 WORDS / SEC.
D84M COMPUTER FOR PERSHING IPTS

CENTRAL DATA PROCESSOR MODULE

4096 WORD MEMORY MODULE

4096 WORD MEMORY MODULE

4096 WORD MEMORY MODULE

EXPANDABLE TO THREE ADDITIONAL MEMORY MODULES

DATA

ADDRESS

CONTROL

DATA

ADDRESS AND TIMING

MODULE INTERFACE CONTROL

SPECIAL I/O LOGIC

DATA AND CONTROL TO NON-TACTICAL DEVICES

DATA AND CONTROL TO TACTICAL DEVICES
D84M COMPUTER WITH CONCURRENT MEMORY ACCESS

- CENTRAL DATA PROCESSOR MODULE
- 4096 WORD MEMORY MODULE
- MODULE INTERFACE CONTROL
- I/O MODULE
  - UNBUFFERED I/O CHANNEL OR SPECIAL I/O LOGIC
- DATA EXCHANGE MODULE
  - UP TO EIGHT INDEPENDENT DATA AND ADDRESS AND TIMING LINES FOR CONCURRENT MEMORY ACCESS
  - UP TO SIX INDEPENDENT DATA AND CONTROL LINES FOR CONCURRENT OPERATION OF SIX HIGH SPEED PERIPHERAL DEVICES

* EIGHT MAX. PER CDP
D84M ASSEMBLER PROGRAM

LANGUAGE: FORTRAN IV (COMPATIBLE WITH IBM 7044, 7094, 360, GE 625)

FEATURES:
47 BASIC INSTRUCTIONS
OVER 300 MNEMONICS
SOFTWARE LITERALS
LIBRARY SUBROUTINES
27 PSEUDO OPERATIONS

INPUT: CARD DECK

OUTPUTS:
HARD COPY
PAPER TAPE FOR LOADING PROGRAMS INTO D84
A) MAGNETIC TAPE TO PREPARE PAPER TAPE
B) CARD DECK TO PREPARE PAPER TAPE
SIMULATOR INPUT PROGRAM
A) MAGNETIC TAPE
B) CARD DECK
SUBROUTINE LIBRARY ON MAGNETIC TAPE

STORAGE REQUIREMENTS: 12,000 WORDS
RUNNING TIME: 6-7 MINUTES (AVERAGE)
D84M SIMULATOR PROGRAM

LANGUAGE: FORTRAN IV (COMPATIBLE WITH IBM 7044, 7094, 360, & GE 625)

FEATURES:
- Simulation of CDP and I/O
- Specifiable memory configuration & cycle time

DEBUGGING AIDS:
- Full or partial trace of program
- Full or partial listing of memory
- Loading of portions of simulated memory during simulation

MONITORING OF ERRORS DURING SIMULATION
RUNNING MORE THAN ONE SIMULATION*
- Simulation of real time
- Simulation of interrupts under operator control

* i.e. Simulating 2 programs in one run.
DIAGNOSTIC PROGRAM

MANUAL PROCEDURES
- POWER-ON
- MODULE SELECTION SWITCHES-OFF
- DIAGNOSTIC SWITCH-ON
- LAMP TEST-CK DRIVER AND LAMPS
- LOAD DIAGNOSTIC TAPE
- MANUAL CK OF TAPE READER

STL TAPE CHECK
- INPUT CHECK: INPUT CIRCUITS FROM READER TO MEMORY
- NIXIE CHECK: LIGHT PATERNs AND DECODING CIRCUITS
- PARITY CHECK: PARITY DECODING CIRCUITS
- COMPARITOR CHECK:
- INITIAL MEMORY CHECK:
- SINGLE INSTRUCTION CHECK: TIMING CHAIN AND OP REG.

ISOLATION IN THIS PHASE 1.45-3.15 MIN.
ISOLATION IN THIS PHASE 4.25 - 6.70 MIN.
D84M DIAGNOSTIC PROGRAM—CONTINUED

DYNAMIC CHECK:

LOAD DIAGNOSTIC PROGRAM IN 4000 WORDS OF MEMORY.

- CHECK CDP
- CHECK I/O
- CHECK MEMORY
- CHECK PERIPHERAL EQUIPMENT

ISOLATION TIMES:

- 7.05 - 7.80 MIN
- 7.25 - 12.25

TOTAL RUN TIME WITHOUT ERROR: 7.50
D84 DIAGNOSTIC PROGRAM VALIDATION

D825 FUNCTIONS
SIMULATE OPERATOR ACTION
INSERT DIAGNOSTIC PROGRAM
INSERT FAULTS IN PROPER SEQUENCE
RECORD RESULTS

D84M
(IN DEBUG RACK)
GATE ELEMENT
POWER VS. PROPAGATION DELAY
(SPEED-POWER TRADEOFFS)

* D84 LOGIC USES >85% LOW-POWER, < 15% HIGH-POWER GATES.

28.
STORAGE ELEMENT
POWER VS. PROPAGATION DELAY

POWER, m watts

PROPAGATION DELAY, n sec

RCTL →
(1 MS)

X MULTIPLIER

X RTL(DR)

X RTL(HI)

X JK

X TTL

X DTL

X SERIES '53
RTL FLIP-FLOP
NEGATIVE LOGIC SYMBOLS
USED IN D84 FOR FLAT PACKS

HIGH POWER LOGIC

HIGH POWER BUFFER
11040622

4 INPUT-HIGH
POWER GATE
11040625

DUAL-2 INPUT-HIGH
POWER GATE
11040624

DUAL-3 INPUT-HIGH
POWER GATE
11040623
NEGATIVE LOGIC SYMBOLS
USED IN D84 FOR FLAT PACKS

LOW POWER LOGIC

4 INPUT-LOW POWER GATE-WITH INVERTER
11040621

DUAL-2 INPUT-LOW POWER GATE
11040620

LOW POWER HALF ADDER-WITH INVERTER
11040617

GATED LOW POWER BUFFER-BL
11040618
NEGATIVE LOGIC SYMBOLS USED IN D84 FOR FLAT PACKS
LOW POWER LOGIC (CONTINUED)

LOW POWER EXPANDER\(^*\) EL
11040615

LOW POWER FLIP-FLOP-FF
11040616

DUAL-3 INPUT-LOW POWER GATE
11040619

\(^*\) USED ON GATE INPUTS, FOR INCREASED FAN-IN WHEN NECESSARY.
MEMORY SYSTEM BLOCK DIAGRAM

INTEGRATED FRONT-END

PLUG-IN ASSEMBLY

DISCRETES

INTEGRATED

SENSE AMPLIFIER

1 ... 25

DATA REGISTER

CDP

DATA OUT

DATA IN

INHIBIT DRIVERS

CORE DRIVERS

DECODING LOGIC

MEMORY ADDRESS:

FROM I/O

CONTROL

INTEGRATED DRIVERS

SELECT MUX

4096-WORD 25-BIT STACK

INTEGRATED CONTROL

DISCRETES INTEGRATED

36.
### RELIABILITY - D84*

<table>
<thead>
<tr>
<th>MODULE</th>
<th>FAILURE RATE</th>
<th>MTBF (HOURS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER SUPPLY</td>
<td>56.58</td>
<td>17,600</td>
</tr>
<tr>
<td>CDP</td>
<td>74.49</td>
<td>13,400</td>
</tr>
<tr>
<td>I/O</td>
<td>77.0 (MIC &amp; I CHANNEL)</td>
<td>13,000</td>
</tr>
<tr>
<td>MEMORY</td>
<td>269.27</td>
<td>3,700</td>
</tr>
<tr>
<td>SYSTEM</td>
<td>477</td>
<td>2,100 HRS.</td>
</tr>
</tbody>
</table>

ESTIMATED IMPROVEMENT VIA MINUTEMAN SELECTION CRITERIA FOR DISCRETE COMPONENTS - 2 TO 2 1/2 TIMES.

* FOR BASIC SYSTEM DEFINED BY "GREEN SHEETS", WITH 4K MEMORY.

90% CONFIDENCE LEVEL.

.003% PER 1000 HRS. I.C. FAILURE RATE (0.03/10^6 HOURS) 37.
CONTAINS:

1  CDP MODULE
1  I/O MODULE
1  4096x25 BIT CORE MEMORY MODULE
1  POWER PACK (NOT PLUGGABLE)

HEIGHT: 13.7 IN.
WIDTH: 12.5 IN.
DEPTH: 15.0 IN.
VOLUME: 1.4 CU. FT.
WEIGHT: 100 LB.
POWER: 110 WATTS
COOLING: NONE

* CONTAINS 4 PLUGGABLE "CARDS", EACH A SANDWICH OF TWO PRINTED CIRCUIT (MOTHER) BOARDS CONTAINING UP TO 48 ("3-D") CIRCUIT NETWORK MODULES.
D84 PROTOTYPE TEST STATION

PROGRAMMER'S PANEL
CIRCUIT NETWORK MODULE FOR D84 PREPRODUCTION PROTOTYPE

HEIGHT: 0.43 IN.
DEPTH: 0.8 IN.
WIDTH: 1.3 IN.

VOLUME: 0.45 CU. IN.
WEIGHT: 30 GRAMS
D84M COMPUTER

HEIGHT: 18.0 IN.
DEPTH: 16.5 IN.
WIDTH: 21.0 IN.

WEIGHT: 150 LB.
VOLUME: 3.9 CU. FT.
POWER: 160 WATTS
COOLING: NONE

* MINIMUM("GREEN SHEET") SYSTEM
I/O AND CDP MODULES

** BACKPLANE --

JACKING DEVICE

85 CNM's MAX.

<table>
<thead>
<tr>
<th></th>
<th>I/O</th>
<th>CDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>HEIGHT</td>
<td>16.0 IN.</td>
<td>16.0 IN.</td>
</tr>
<tr>
<td>WIDTH</td>
<td>6.0 IN.</td>
<td>6.0 IN.</td>
</tr>
<tr>
<td>DEPTH</td>
<td>14.5 IN.</td>
<td>14.5 IN.</td>
</tr>
<tr>
<td>VOLUME</td>
<td>0.78 CU. FT.</td>
<td>0.78 CU. FT.</td>
</tr>
<tr>
<td>WEIGHT</td>
<td>APPLICATION</td>
<td>50 LB.</td>
</tr>
<tr>
<td></td>
<td>DEPENDENT</td>
<td>43 WATTS</td>
</tr>
</tbody>
</table>

* MOVES MODULE TO MATE WITH SHEAR PINS, AND GUIDE TO FLOATING CONNECTORS.

** MAX. OF 3 WIRES/PIN - SOLDERED OR WIRE-WRAPPED AT CUSTOMER'S OPTION.
D84M CIRCUIT NETWORK MODULE (CNM)

HEIGHT: 0.25 IN.
DEPTH: 6.5 IN.
WIDTH: 1.5 IN.
VOLUME: 2.5 CU. IN.
WEIGHT: 26 GRAMS

PC BOARD, DIP-SOLDERED TO CONNECTORS ON ALUMINUM EXTRUDED FRAME.
MEMORY MODULE

STACK, WITH DIODES, — 2 1/4" W. X 3 1/4" D. X 6" H.

OVER-WIDTH CNM, TO ACCOMMODATE DISCRETES

26 CNM LOCATIONS

HEIGHT : 8.0 IN.
DEPTH : 14.5 IN.
WIDTH : 3.9 IN.

WEIGHT : 13 LB.
VOLUME : 0.26 CU. FT.
POWER : 75 WATTS ACTIVE*
12 WATTS STANDBY

* WORST-CASE, WHEN WRITING ALL 0's EACH MEMORY CYCLE.
POWER PACK

HEIGHT: 16.0 IN.  WEIGHT: 35 LB.
DEPTH: 14.5 IN.  VOLUME: 0.52 CU. FT.
WIDTH: 4.5 IN.  POWER CAPACITY: 300 WATTS

DISCRETE COMPONENTS, ALL ON REMOVABLE SUB-ASSEMBLIES
MOUNTING BASE ASSEMBLY

REMovable BACKBOARD • INTER-MODULE WIRING ACCESSIBLE FROM REAR •

HEIGHT : 18.0 IN.  WIDTH*: 30.0 IN.
DEPTH : 16.5 IN.  WEIGHT*: 41 LB.

* THIS ASSEMBLY PROVIDES FOR 24K MEMORY

46.
TYPICAL D84M CONFIGURATIONS

CONTAINS: ①
1 CDP MODULE
1 I/O MODULE
2 4096 x 25 BIT MEMORY MODULES
1 MAGNETIC TAPE CONTROLLER
1 POWER PACK

CONTAINS: ②
1 CDP MODULE
1 I/O MODULE
3 4096 x 25 BIT MEMORY MODULES
1 POWER PACK
PROVISIONS FOR EXPANSION TO 24K MEMORY

HEIGHT: 18.0 IN.
WIDTH: 25.0 IN.
DEPTH: 16.5 IN.
VOLUME: 4.5 CU.FT.
WEIGHT: 210 LB.
POWER: 230 WATTS* 

HEIGHT: 18.0 IN.
WIDTH: 30.0 IN.
DEPTH: 16.5 IN.
VOLUME: 5.25 CU.FT.
WEIGHT: 218 LB.
POWER: 230 WATTS*

* ONE 4096-WORD MEMORY ACTIVE, BALANCE ON STANDBY—WORST CASE

① SYSTEM BLOCK DIAGRAM ON CHART 21.
② SYSTEM BLOCK DIAGRAM ON CHART 20.
D84A AIRBORNE COMPUTER

MULTI-LAYER BOARD-CONNECTOR PINS BETWEEN LAMINATES; ALLOWS 0.150" CNM PITCH VS. 0.250" PITCH IN D84M.

CONTAINS:

1 CDP MODULE
1 I/O MODULE
1 4096 x 25 BIT CORE MEMORY MODULE
1 POWER PACK

HEIGHT: 7 5/8 IN.
WIDTH: 15 3/8 IN.
DEPTH: 19 9/16 IN.
WEIGHT: 60 LB.
POWER: 170 WATTS
COOLING: 30 CFM (AT SEA LEVEL)

D84A AND D84M CNM's ARE LOGICALLY IDENTICAL, TYPE FOR TYPE.
CONTAINS:

<table>
<thead>
<tr>
<th>D84 M</th>
<th>D84 A</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 CDP MODULE</td>
<td>15 7/8 IN.</td>
</tr>
<tr>
<td>1 I/O MODULE</td>
<td>15 3/8 IN.</td>
</tr>
<tr>
<td>1 POWER PACK</td>
<td>19 9/16 IN.</td>
</tr>
<tr>
<td>3 4096-WORD MEMORY MODULES</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>D84 M</th>
<th>D84 A</th>
</tr>
</thead>
<tbody>
<tr>
<td>HEIGHT:</td>
<td>18.0 IN.</td>
<td>15 7/8 IN.</td>
</tr>
<tr>
<td>WIDTH:</td>
<td>30.0 IN.</td>
<td>15 3/8 IN.</td>
</tr>
<tr>
<td>DEPTH:</td>
<td>16.5 IN.</td>
<td>19 9/16 IN.</td>
</tr>
<tr>
<td>WEIGHT:</td>
<td>218 LB.</td>
<td>88 LB.</td>
</tr>
<tr>
<td>VOLUME:</td>
<td>5.25 CU.FT.</td>
<td>2.66 CU.FT.</td>
</tr>
<tr>
<td>POWER</td>
<td>230 WATTS</td>
<td>194 WATTS</td>
</tr>
<tr>
<td>IN SAME VOLUME</td>
<td>3 MORE 4096-WORD</td>
<td>1 MORE 4096-WORD</td>
</tr>
<tr>
<td>MEMORIES</td>
<td>MEMORIES ACCOMMODATED</td>
<td>MEMORIES ACCOMMODATED</td>
</tr>
<tr>
<td>ACCOMMODATED</td>
<td>(FOR 24 K TOTAL)</td>
<td>(FOR 16 K TOTAL)</td>
</tr>
</tbody>
</table>
D84A SYSTEM EXPANSION

BASIC COMPUTER

EXAMPLES OF MODULE MIXES FOR SYSTEM EXPANSION

WT. EA.

P. S. 13 LB. 13 13
4K MEM. 6 LB. 6 6 6 12 18
I/O (FULL) 13 LB. 13 13 13 13
CDP 12 LB. 12 12
ATR 16 LB. 16 16 16 16
DEM 12 LB. 12

50.
TYPICAL CONTROL AND MAINTENANCE EQUIPMENT

- MAINTENANCE PANEL
- PHOTOELECTRIC PAPER TAPE READER
- SPECIAL PANEL
SOFTWARE—LATER DELIVERIES
(2nd. HALF —'66)

1. ON—LINE ASSEMBLER
   - 2 PASS ON MINIMUM SYSTEM
   - RELOCATABLE SUBROUTINES

2. COMPILER
   - FORTRAN IV

3. EXECUTIVE PROGRAM
   - LOADER, ON MINIMUM SYSTEM
   - MULTIPROCESSING
NEW SPECIFICATION SHEETS TO BE RELEASED: DELIVERY CAPABILITY

DATA EXCHANGE MODULES — 3 TYPES

1— TO ADDRESS 65K HOMOGENEously
2— TO BUFFER WITH CONCURRENT ACCESS TO MEMORY
   BY I/O AND CDP (AND INCLUDE (1))
3— TO MULTI-PROCESS (AND INCLUDE 1 AND 2)

BUFFERING OPTIONS 1st & 2nd QUARTER '66

D84A PACKAGING OPTION 3rd QUARTER '66

CONTROLLER LOGIC FOR COMMONLY USED PERIPHERALS 1st QUARTER '66

I/O EXCHANGE OPTION ON EACH CONTROLLER TYPE 2nd QUARTER '66

NDRO THIN FILM 1st QUARTER '67

CHARACTER MANIPULATION 2nd QUARTER '66

BINARY<->BCD CONVERSION HARDWARE 2nd QUARTER '66

53,
BUDGETARY PRICES

"GREEN SHEET MACHINE" – D84M OR D84A
PACKAGING – WITH 4K MEMORY

1 – $96K ($74K)
10 – $70K ($55K)
100 – $57K ($52K)
500 – $48K ($48K)

ADDITIONAL MEMORY MODULES

1 – $19K ($17K)
10 – $15K ($14K)
100 – $12K ($12K)
500 – $10K ($10K)

PRICES IN PARENTHESES ARE FOR LIMITED ENVIRONMENT – FROM +15°C TO +55°C